L Number	Hits	Search Text	DB	Time stamp
1	1	("6051849").PN.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/11/14 14:41
2	4	(("6177688") or ("5880485") or ("6153010") or ("6325850")).PN.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/11/14 14:42
-	32207	(elog log lateral adj overgrow$2) and (gallium near5 nitride gan (ga near10 al near "10" n) (ga near10 n))	USPAT; EPO; JPO	2003/11/13 17:40
-	375	(elog log lateral adj overgrow$2) and (iii-v gallium near5 nitride gan)	USPAT; EPO; JPO	2001/11/03 12:10
-	372	(elog log lateral adj overgrow$2) and (iii-v gallium near5 nitride gan) not gan.in.	USPAT; EPO; JPO	2001/11/03 12:10
-	223	(elog log lateral adj overgrow$2) and (iii-v gallium near5 nitride gan) not gan.in. and (w tungsten)	USPAT; EPO; JPO	2001/11/03 12:14
-	48	(elog log lateral adj overgrow$2) and (iii-v gallium near5 nitride gan) not gan.in. and (tungsten)	USPAT; EPO; JPO	2001/11/03 12:14
-	9	("5073230" | "5328549" | "5376229" | "5683596" | "5710057").PN.	USPAT; EPO; JPO	2001/11/03 12:20
-	305	(elog log lateral adj overgrow$2) and (gallium near10 nitride gan)	USPAT; EPO; JPO	2003/02/06 16:15
-	162	arcsec arcseconds	USPAT; EPO; JPO	2003/02/06 16:12
-	288	arcsec arcseconds arc-sec arc-seconds	USPAT; EPO; JPO	2003/11/13 17:57
-	1	((elog log lateral adj overgrow$2) and (gallium near10 nitride gan)) and (arcsec arcseconds arc-sec arc-seconds)	USPAT; EPO; JPO	2003/02/06 16:13
-	6	("5332697" | "5888886" | "5900650" | "5929466" | "6030848" | "6090666").PN.	USPAT	2003/02/06 16:14
-	7698	gallium near10 nitride gan	USPAT; EPO; JPO	2003/02/06 16:15
-	22	(gallium near10 nitride gan) and (arcsec arcseconds arc-sec arc-seconds)	USPAT; EPO; JPO	2003/02/06 16:18
-	4	"(0004)" near2 reflection	USPAT; EPO; JPO	2003/11/13 17:50
-	468	(elog log lateral adj overgrow$2) and (iii-n gallium near5 nitride gan (ga near10 al near10 n) (ga near10 n))	USPAT; EPO; JPO	2003/11/13 18:07
-	4	"(0004)" near2 reflection	USPAT; EPO; JPO	2003/11/13 17:40
-	314	arcsec arcseconds arc-sec arc-seconds	USPAT; EPO; JPO	2003/11/13 17:45
-	13983	fwhm half near2 (max maximum) (x-ray rocking) near2 curve	USPAT; EPO; JPO	2003/11/13 17:55
-	77	(arcsec arcseconds arc-sec arc-seconds) and (fwhm half near2 (max maximum) (x-ray rocking) near2 curve)	USPAT; EPO; JPO	2003/11/13 17:46
-	2	((elog log lateral adj overgrow$2) and (iii-n gallium near5 nitride gan (ga near10 al near10 n) (ga near10 n))) and ((arcsec arcseconds arc-sec arc-seconds) and (fwhm half near2 (max maximum) (x-ray rocking) near2 curve))	USPAT; EPO; JPO	2003/11/13 17:46
-	6	("5332697" | "5888886" | "5900650" | "5929466" | "6030848" | "6090666").PN.	USPAT	2003/11/13 17:48
-	5	("5272108" | "5874747" | "5877038" | "5930656" | "5977566").PN.	USPAT	2003/11/13 17:49
-	9	"(0004)" with gan	USPAT; EPO; JPO	2003/11/13 17:50
-	13983	fwhm "(fwhm)" half near2 (max maximum) (x-ray rocking) near2 curve	USPAT; EPO; JPO	2003/11/13 17:56
-	1374884	arcsec arcseconds arc-sec arc-seconds degree degrees seconds	USPAT; EPO; JPO	2003/11/13 17:57

-	15	((elog log lateral adj overgrow$2) and (iii-n gallium near5 nitride gan (ga near10 al near10 n) (ga near10 n))) and (fwhm "(fwhm)" half near2 (max maximum) (x-ray rocking) near2 curve) and (arcsec arcseconds arc-sec arc-seconds degree degrees seconds)	USPAT; EPO; JPO	2003/11/13 18:03
-	2283	(428/698).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/11/13 18:03
-	253	(428/642).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/11/13 18:06
-	410	(257/190).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/11/13 18:07
-	0	(elog log lateral adj overgrow$2) and (((428/698).CCLS.) ((428/642).CCLS.) ((257/190).CCLS.)) and (fwhm "(fwhm)" half near2 (max maximum) (x-ray rocking) near2 curve)	USPAT; EPO; JPO	2003/11/14 14:39

US006153010A

United States Patent [19]

Kiyoku et al.

[11] Patent Number: 6,153,010

[45] Date of Patent: Nov. 28, 2000

[54] **METHOD OF GROWING NITRIDE SEMICONDUCTORS, NITRIDE SEMICONDUCTOR SUBSTRATE AND NITRIDE SEMICONDUCTOR DEVICE**

[75] Inventors: **Hiroyuki Kiyoku; Shuji Nakamura; Tokuya Kozaki; Naruhito Iwasa; Kazuyuki Chocho**, all of Anan, Japan

[73] Assignee: **Nichia Chemical Industries Ltd.**, Tokushima-ken, Japan

[21] Appl. No.: **09/202,141**

[22] PCT Filed: **Apr. 9, 1998**

[86] PCT No.: **PCT/JP98/01640**

§ 371 Date: **Dec. 9, 1998**

§ 102(e) Date: **Dec. 9, 1998**

[87] PCT Pub. No.: **WO98/47170**

PCT Pub. Date: **Oct. 22, 1998**

[30] **Foreign Application Priority Data**

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Jun. 30, 1997	[JP]	Japan	9-174494
Jul. 7, 1997	[JP]	Japan	9-181071
Jul. 28, 1997	[JP]	Japan	9-201477
Oct. 9, 1997	[JP]	Japan	9-277448
Oct. 22, 1997	[JP]	Japan	9-290098
Nov. 26, 1997	[JP]	Japan	9-324997

[51] **Int. Cl.**[7] **C30B 23/04**; C30B 25/04

[52] **U.S. Cl.** **117/95**; 117/97; 117/106; 117/952

[58] **Field of Search** 117/84, 88, 89, 117/91, 101, 102, 104, 105, 952, 95, 97, 106

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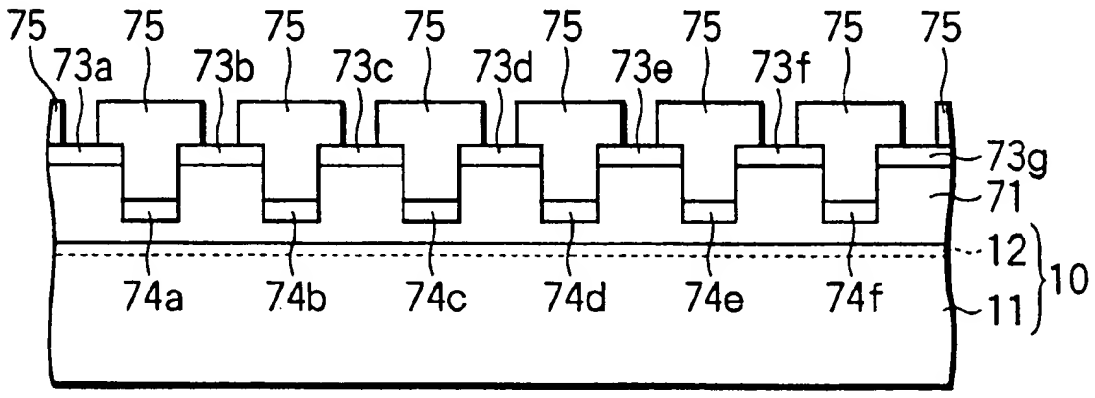
Primary Examiner—Benjamin L. Utech
Assistant Examiner—Matt Anderson
Attorney, Agent, or Firm—Nixon & Vanderhye

[57] **ABSTRACT**

A method of growing a nitride semiconductor crystal which has very few crystal defects and can be used as a substrate is disclosed. This invention includes the step of forming a first selective growth mask on a support member including a dissimilar substrate having a major surface and made of a material different from a nitride semiconductor, the first selective growth mask having a plurality of first windows for selectively exposing the upper surface of the support member, and the step of growing nitride semiconductor portions from the upper surface, of the support member, which is exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the nitride semiconductor portions grown in the adjacent windows combine with each other on the upper surface of the selective growth mask.

30 Claims, 8 Drawing Sheets



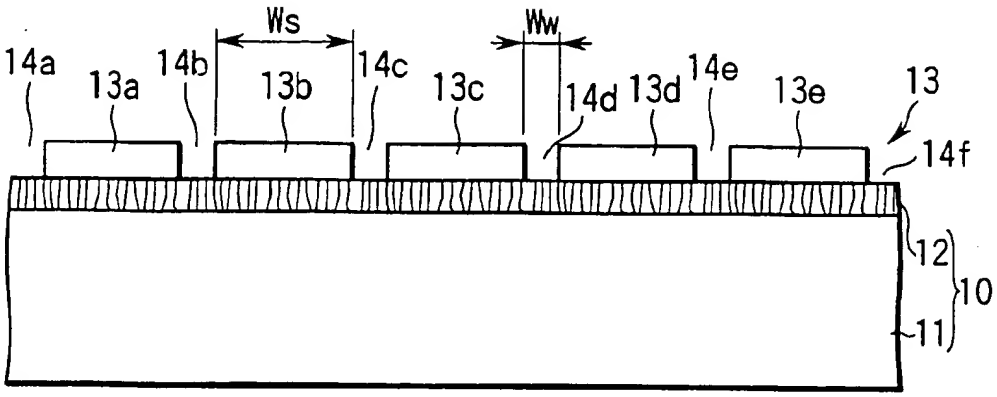


FIG. 1A

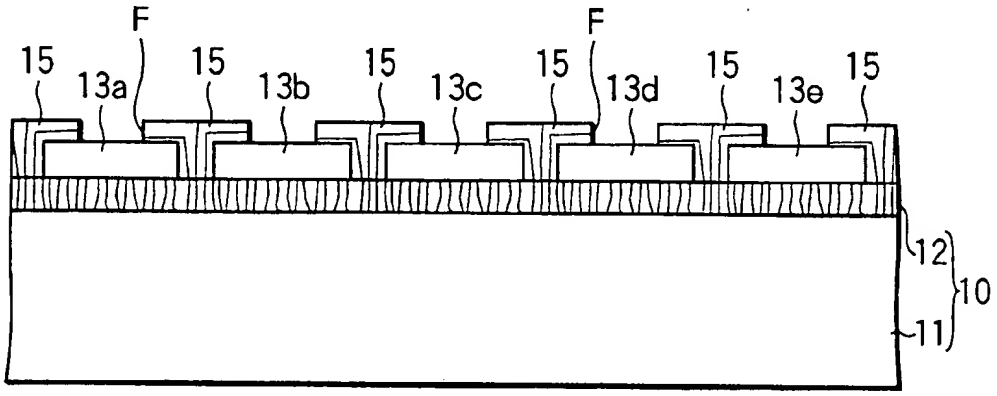


FIG. 1B

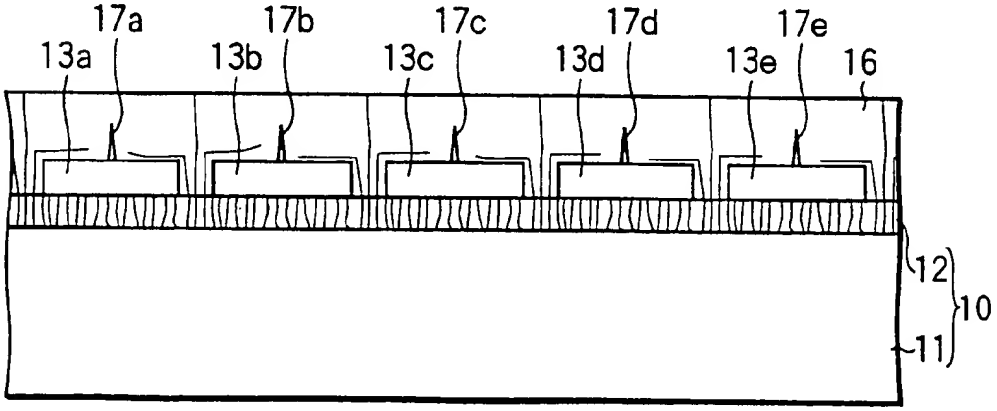


FIG. 1C

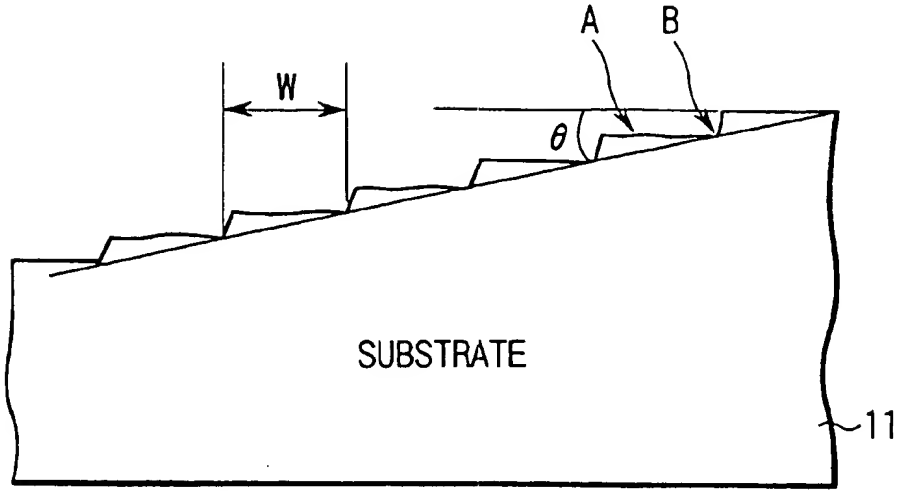

A
B
W
θ
SUBSTRATE
11

FIG. 2

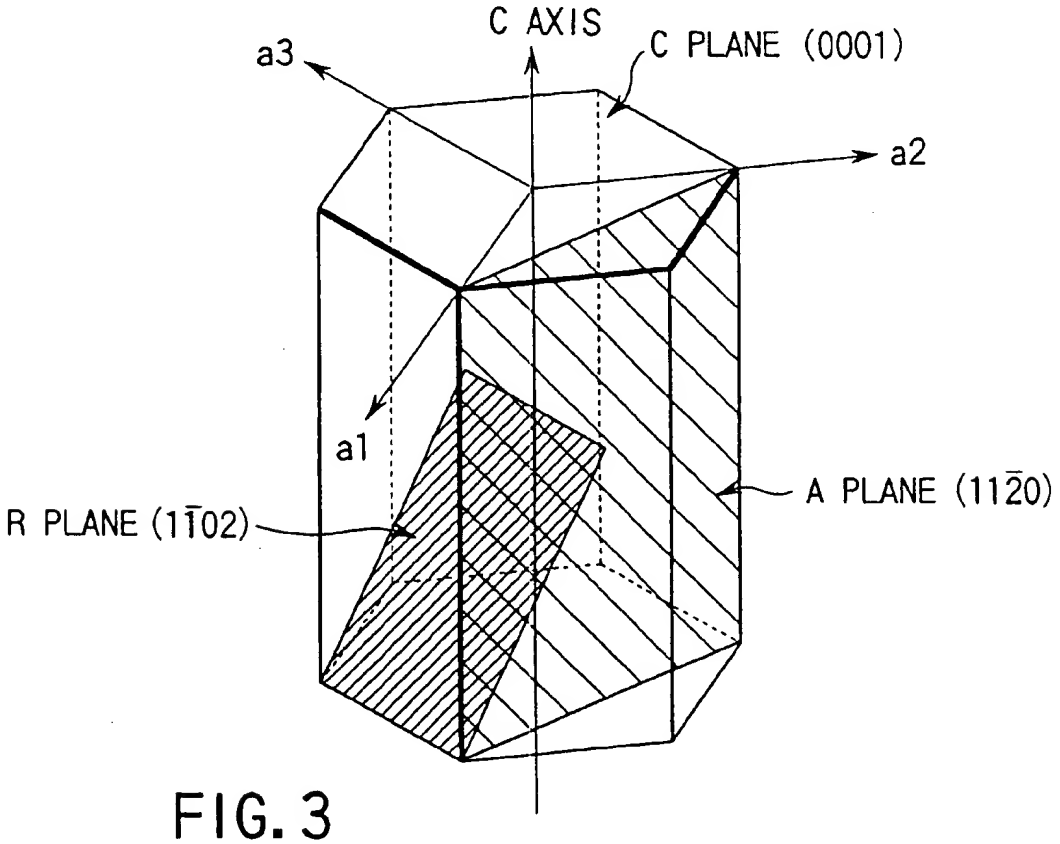

C AXIS
C PLANE (0001)
a3
a2
a1
R PLANE (1$\bar{1}$02)
A PLANE (11$\bar{2}$0)

FIG. 3

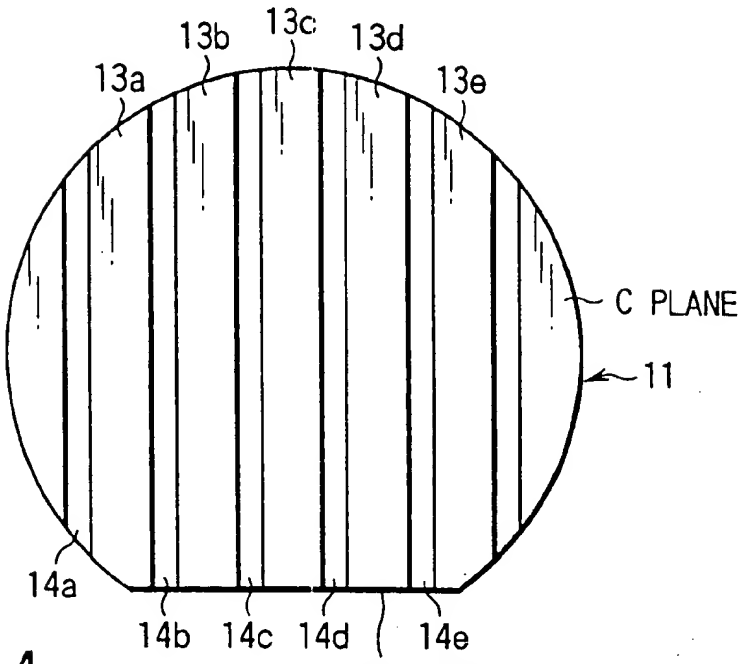


FIG. 4

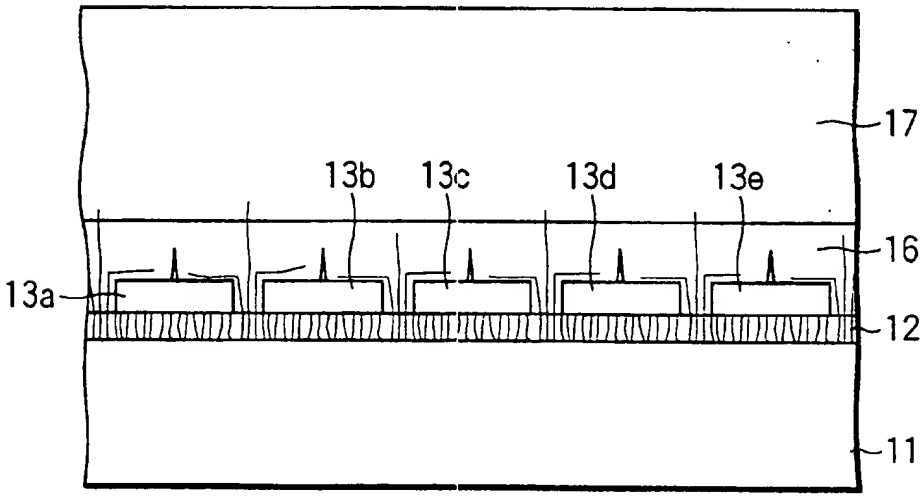


FIG. 5A

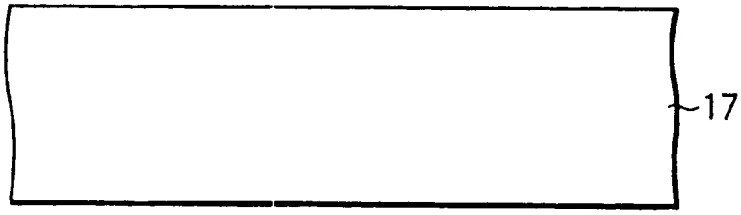


FIG. 5B

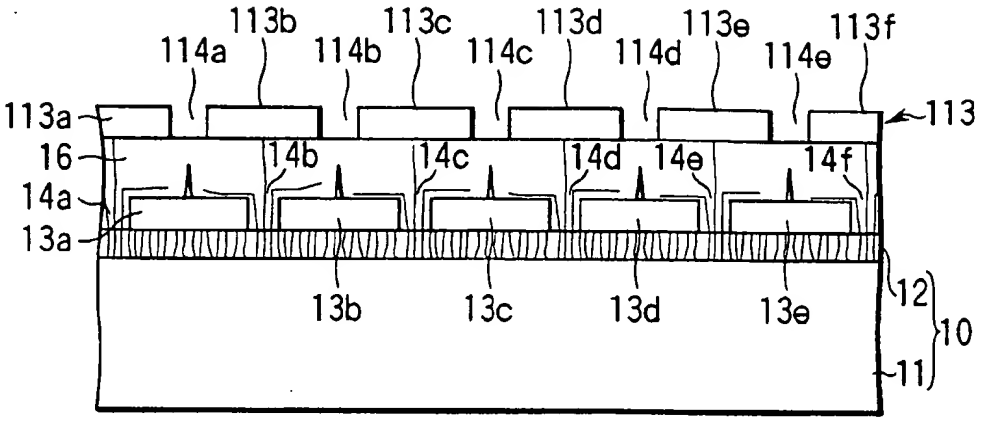


FIG. 6A

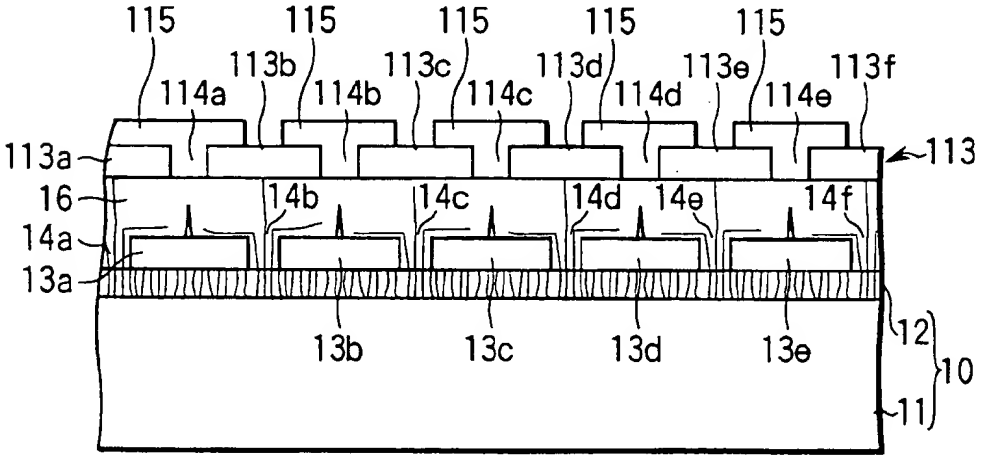


FIG. 6B

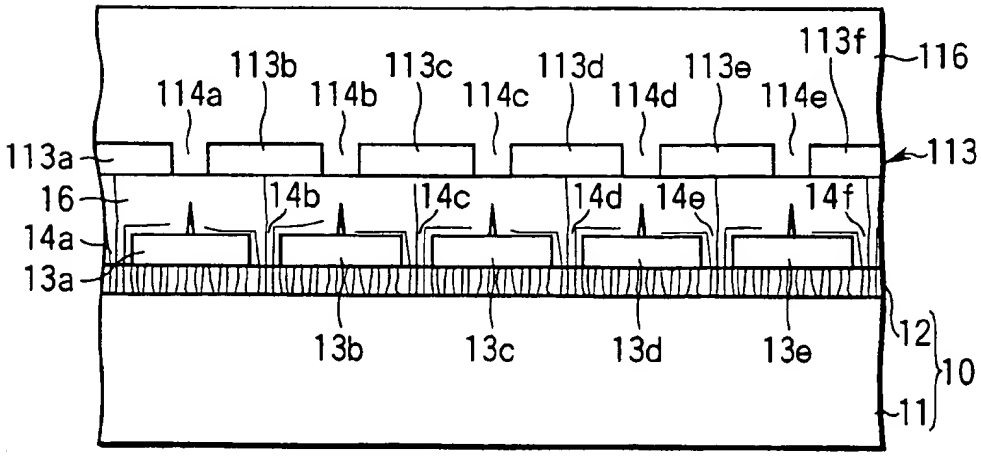


FIG. 6C

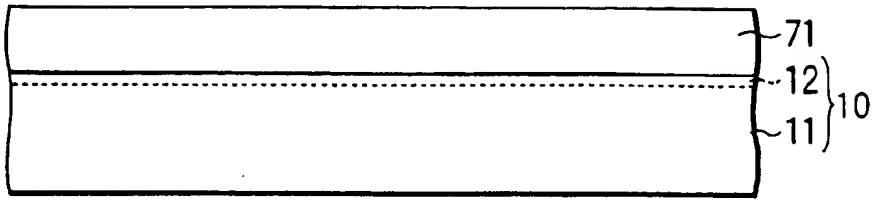


FIG. 7A

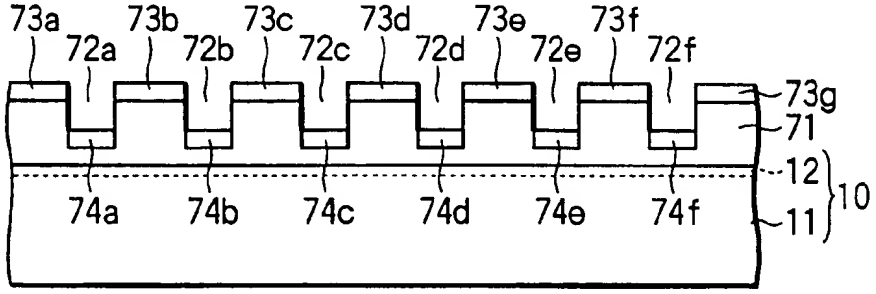


FIG. 7B

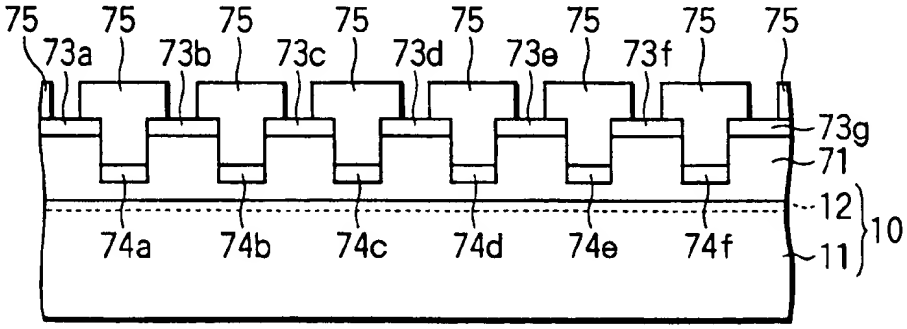


FIG. 7C

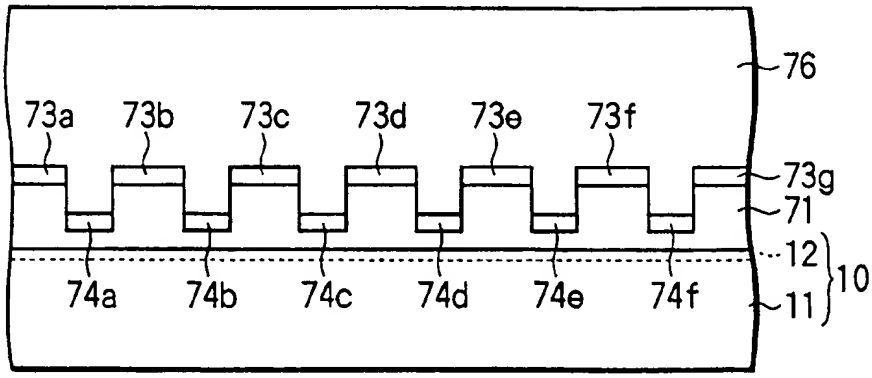


FIG. 7D

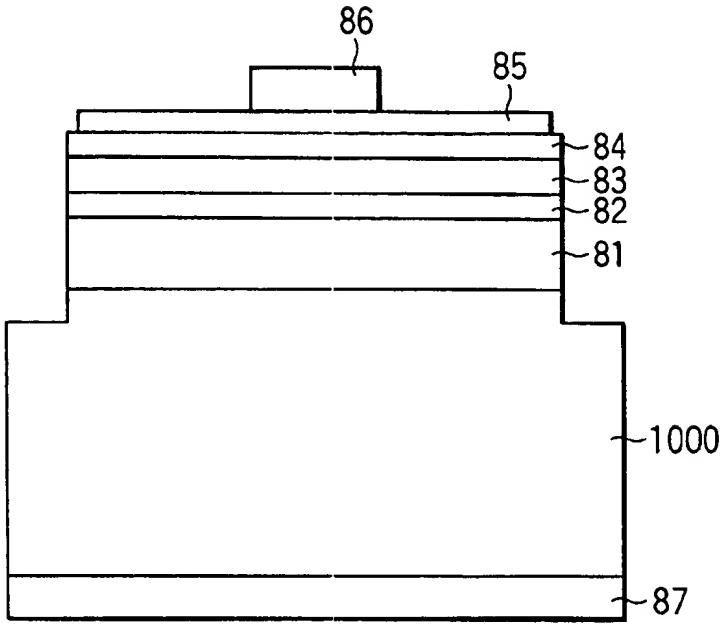


FIG. 8A

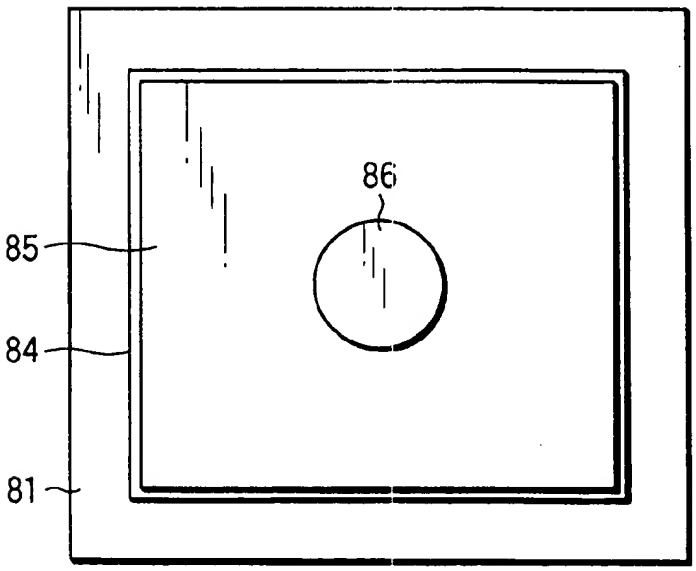


FIG. 8B

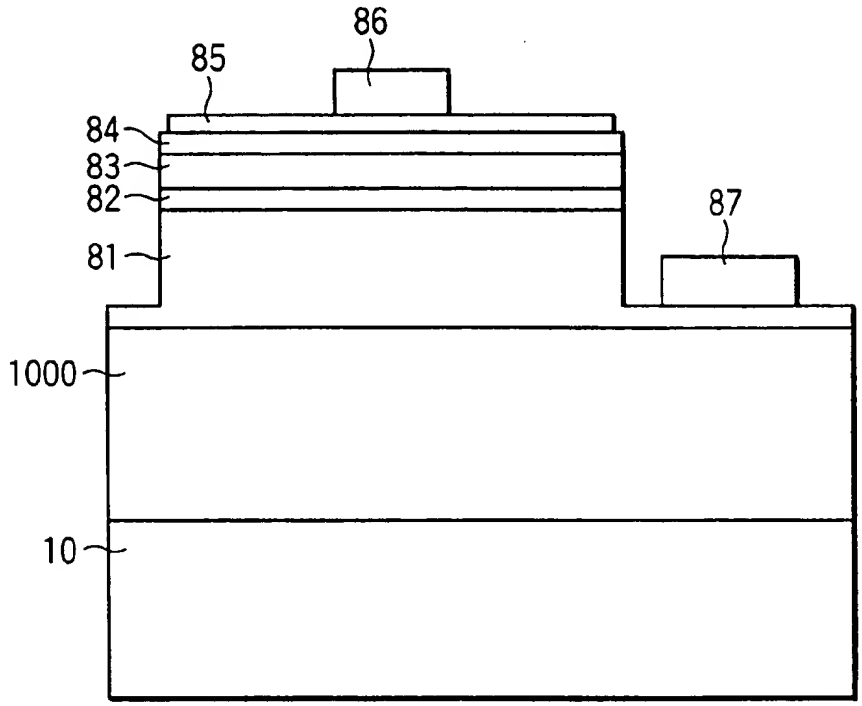

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FIG. 9

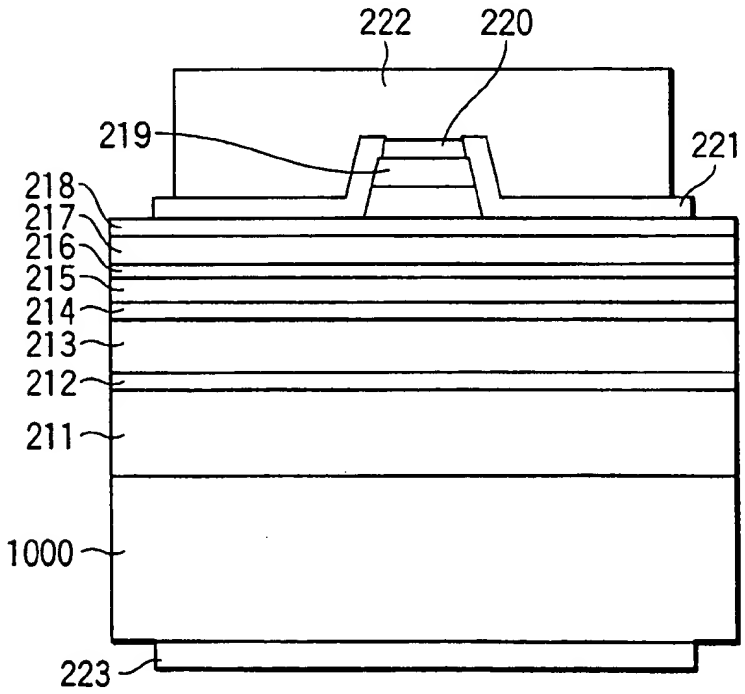
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FIG. 10

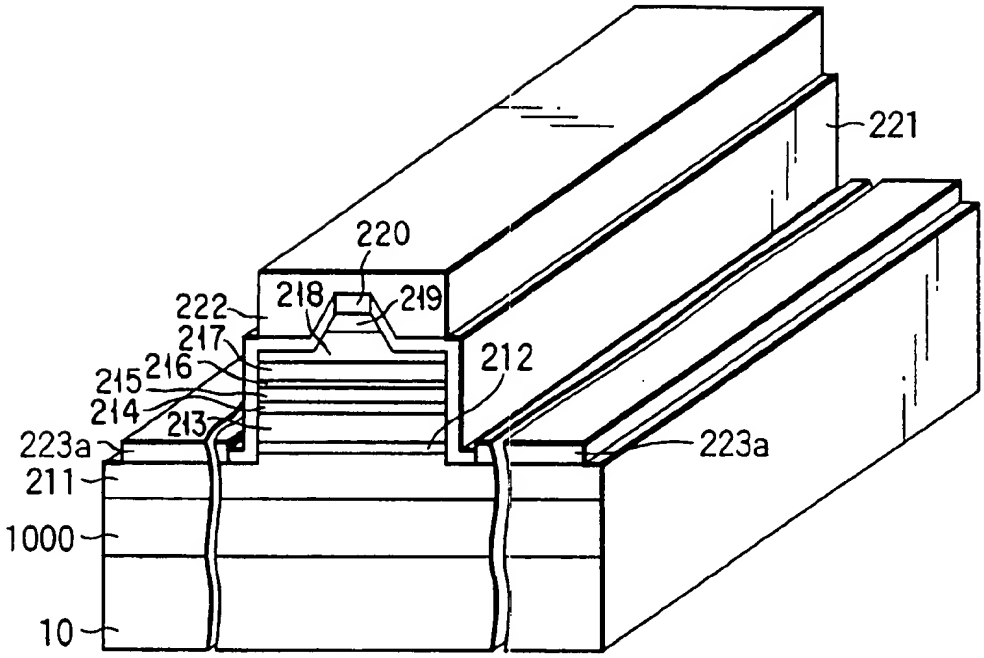
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FIG. 11

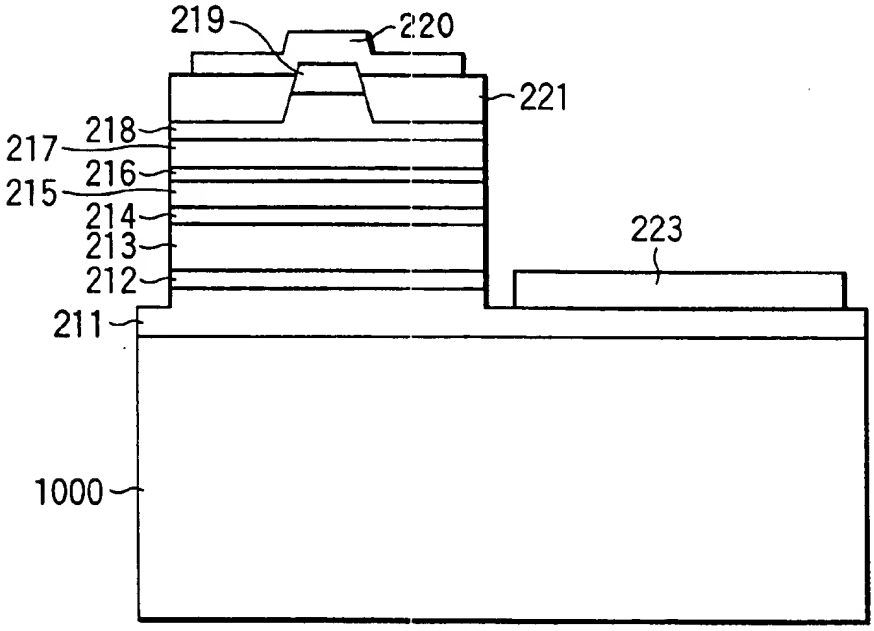
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FIG. 12

METHOD OF GROWING NITRIDE SEMICONDUCTORS, NITRIDE SEMICONDUCTOR SUBSTRATE AND NITRIDE SEMICONDUCTOR DEVICE

TECHNICAL FIELD

The present invention relates to a nitride semiconductor growth method, a nitride semiconductor substrate, and a nitride semiconductor device and, more particularly, to a method of growing a nitride semiconductor having good crystal quality by using a substrate made of a material different from a nitride semiconductor, a nitride semiconductor substrate, and a nitride semiconductor device.

BACKGROUND ART

It is generally known that a semiconductor having few crystal defects and good crystallinity is grown on a substrate by using a substrate lattice-matched with the semiconductor to be grown. There is, however, no substrate that is lattice-matched with a nitride semiconductor, has excellent crystallinity, and allows a nitride semiconductor crystal to be stably grown. For this reason, there is no choice but to grow a nitride semiconductor on a substrate, e.g., a sapphire, spinnel, or silicon carbide substrate, that is not lattice-matched with nitride semiconductors.

Various research institutes have made attempts to manufacture GaN bulk crystals that are lattice-matched with nitride semiconductors. However, it has only been reported that GaN bulk crystals having sizes of several millimeters are obtained. That is, any practical GaN bulk crystal like the one from which many wafers are cut to be actually used as substrates for the growth of nitride semiconductor layers has not been obtained.

As a technique of manufacturing GaN substrates, for example, Jpn. Pat. Appln. KOKAI Publication Nos. 7-202265 and 7-165498 disclose a technique of forming a ZnO buffer layer on a sapphire substrate, growing a nitride semiconductor on the ZnO buffer layer, and dissolving and removing the ZnO buffer layer. However, since the ZnO buffer layer grown on the sapphire substrate has poor crystallinity, it is difficult to obtain a nitride semiconductor crystal having good quality by growing a nitride semiconductor on the buffer layer. In addition, it is difficult to continuously grow a nitride semiconductor thick enough to be used as a substrate on the thin ZnO buffer layer.

When a nitride semiconductor electronic element used for various electronic devices such as a light-emitting diode (LED) device, a laser diode (LD) device, and a light-receiving device is to be manufactured, if a substrate made of a nitride semiconductor having few crystal defects can be manufactured, a new nitride semiconductor having few lattice defects and forming a device structure can be grown on the substrate. Therefore, the obtained device acquires greatly improved performance. That is, a high-performance device that has not been realized in the past can be realized.

It is, therefore, an object of the present invention to provide a method of growing a nitride semiconductor crystal having excellent crystallinity.

More specifically, it is an object of the present invention to provide a method of growing a nitride semiconductor crystal that can provide a nitride semiconductor substrate, a nitride semiconductor substrate, and a nitride semiconductor device formed on the nitride semiconductor substrate.

DISCLOSURE OF INVENTION

According to a first aspect of the present invention, there is provided a nitride semiconductor growth method comprising the steps of (a) forming a first selective growth mask on a support member made up of a dissimilar substrate made of a material different from a nitride semiconductor and having a major surface, and an underlayer made of a nitride semiconductor formed on the major surface of the dissimilar substrate, the first selective growth mask having a plurality of first windows selectively exposing an upper surface of the underlayer of the support member, and (b) growing nitride semiconductor portions from the upper surface portions, of the underlayer, which are exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the nitride semiconductor portions grown in the adjacent windows combine or unite with each other on an upper surface of the selective growth mask. In this case, the total area of upper surfaces of portions, of the underlayer, which are covered with the first selective growth mask is preferably larger than that of portions, of the underlayer, which are exposed from the first windows.

According to a second aspect of the present invention, there is provided a nitride semiconductor growth method comprising the steps of (a) forming a first selective growth mask on a support member comprising a dissimilar substrate made of a material different from a nitride semiconductor and having a major surface, the first selective growth mask having a plurality of first windows for partly exposing an upper surface of the support member, such that a total area of upper surfaces of portions, of the support member, which are covered with the first selective growth mask is larger than that of portions, of the support member, which are exposed from the first windows, and (b) growing first nitride semiconductor portions from the upper surface portions, of the support member, which are exposed from the windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the nitride semiconductor portions grown in the adjacent windows combine or unite with each other on an upper surface of the selective growth mask.

In the first and second aspects of the present invention, the first selective growth mask is preferably made up of a plurality of individual or discrete stripes spaced apart from each other, defining the first windows therebetween, and extending parallel to each other. In addition, in the first and second aspects, the ratio of a width of each of the stripes to a width of each of the first windows is preferably more than 1 and not more than 20. In the first and second aspects, it is especially preferable that the dissimilar substrate be a sapphire substrate having a major surface forming a (0001) plane, and the respective stripes preferably extend in a direction perpendicular to a $(11\bar{2}0)$ plane of sapphire; the dissimilar substrate be a sapphire substrate having a major surface forming a $(11\bar{2}0)$ plane, and the respective stripes extend in a direction perpendicular to the $(1\bar{1}20)$ plane of sapphire; or the dissimilar substrate be a spinnel substrate having a major surface forming a (111) plane, and the respective stripes extend in a direction perpendicular to the (110) plane of spinnel.

Furthermore, in the first and second aspects, growth of the first nitride semiconductor crystal in the step (b) can be performed by metalorganic vapor-phase epitaxy, and a second nitride semiconductor crystal can be grown, on the grown first nitride semiconductor crystal, by a halide vapor-phase epitaxial growth method. Alternatively, the first and second aspects can further comprise the step (c) of forming a second selective growth mask on the first nitride semiconductor grown in the step (b), the second selective growth mask having a plurality of second windows selectively exposing an upper surface of the first nitride semiconductor, and the step (d) of growing second nitride semiconductor

portions from the upper surface portions, of the first nitride semiconductor, which are exposed from the second windows, by using a gaseous Group 3 element source and a gaseous nitrogen source, until the second nitride semiconductor portions grown in the adjacent windows combine or unite with each other on an upper surface of the second selective growth mask. In this case, the second selective growth mask preferably has the same arrangement or construction as that of the first selective growth mask.

According to a third aspect of the present invention, there is provided a nitride semiconductor growth method comprising the steps of (a) forming a nitride semiconductor layer on a support member comprising a dissimilar substrate made of a material different from a nitride semiconductor and having a major surface, (b) forming a plurality of recess portions having bottom surfaces substantially parallel to an upper surface of the support member in the nitride semiconductor layer, (c) selectively forming a first growth control mask on a top surface of the nitride semiconductor layer to selectively expose the nitride semiconductor layer from side surfaces of the recess portions, and (d) growing a nitride semiconductor from an exposed surface of the nitride semiconductor layer by using a gaseous Group 3 element source and a gaseous nitrogen source. In this case, the first growth control mask preferably has the same arrangement or construction as that of the first selective growth mask in the first and second aspects.

In the third aspect, it is especially preferable that the step (c) further comprise forming a second growth control mask on the bottom surfaces of the recess portions to selectively expose the nitride semiconductor layer from side surfaces of the recess portions. In this case, the first growth control mask is preferably made up of a plurality of individual or discrete stripes spaced apart from each other, defining the first windows therebetween, and extending parallel to each other. In addition, it is especially preferable that the dissimilar substrate be a sapphire substrate having a major surface forming a (0001) plane, and the respective individual stripes extend in a direction perpendicular to a $(11\bar{2}0)$ plane of sapphire; the dissimilar substrate be a sapphire substrate having a major surface forming a $(11\bar{2}0)$ plane, and the respective individual stripes extend in a direction perpendicular to the $(1\bar{1}20)$ plane of sapphire; or the dissimilar substrate be a spinnel substrate having a major surface forming a (111) plane, and the respective stripes extend in a direction perpendicular to the (110) plane of spinnel.

In growing a nitride semiconductor crystal according to the present invention, the gaseous nitrogen source and the gaseous Group III element source are preferably supplied at a molar ratio of not more than 2,000.

In addition, according to the present invention, there is provided a nitride semiconductor substrate comprising a nitride semiconductor crystal and having first and second major surfaces, wherein a region near the first major surface has a relatively small number of crystal defects, and a region near the second major surface has a relatively large number of crystal defects. There is also provided a nitride semiconductor substrate comprising a nitride semiconductor crystal and having first and second major surfaces, characterized by the number of crystal defects in a surface region in the first major surface being not more than $1\times10^5/cm^2$.

Furthermore, according to the present invention, there is provided a nitride semiconductor device comprising a nitride semiconductor device structure supported on the nitride semiconductor substrate of the present invention.

Further developments of the present invention are described in the following description and the appended claims.

In the present invention, a nitride semiconductor can be represented by the formula, $In_aAl_yGa_{1-a-b}N$ (wherein $0\leqq a$, $0\leqq b$, and $a+b\leqq 1$).

BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1A**, **1B**, **1C** are schematic sectional views for explaining the principle of a nitride semiconductor growth method according to the first or second aspect of the present invention in the order of the steps;

FIG. **2** is a schematic sectional view showing a substrate which has an off-angled major surface and can be used to grow a nitride semiconductor layer in accordance with the present invention;

FIG. **3** is a view of a unit cell showing the crystal structure of a nitride semiconductor;

FIG. **4** is a plan view showing a support member on which a striped-shaped selective growth mask is formed;

FIGS. **5A** and **5B** are schematic sectional views for explaining a nitride semiconductor growth method according to another embodiment of the present invention;

FIGS. **6A**, **6B**, **6C** are schematic sectional views for explaining a nitride semiconductor growth method according to still another embodiment of the present invention in the order of the steps;

FIGS. **7A**, **7B**, **7C**, **7D** are schematic sectional views for explaining the principle of a nitride semiconductor growth method according to the third aspect of the present invention in the order of the steps;

FIG. **8A** is a sectional view schematically showing a nitride semiconductor light-emitting diode device supported on a nitride semiconductor substrate of the present invention;

FIG. **8B** is a plane view of the light-emitting diode device in FIG. **8A**;

FIG. **9** is a sectional view schematically showing another nitride semiconductor light-emitting diode device supported on a nitride semiconductor substrate of the present invention;

FIG. **10** is a sectional view schematically showing a nitride semiconductor laser diode device supported on a nitride semiconductor substrate of the present invention;

FIG. **11** is a partially sectional perspective view schematically showing another nitride semiconductor laser diode device supported on a nitride semiconductor substrate of the present invention; and

FIG. **12** is a sectional view schematically showing still another nitride semiconductor laser diode device supported on a nitride semiconductor substrate of the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

The present invention will be described below with reference to the accompanying drawings. The same or similar parts are denoted by the same reference numerals throughout the drawings.

FIGS. **1A** to **1C** are sectional views for explaining the principle of a nitride semiconductor growth method according to the first aspect of the present invention in the order of the steps.

As shown in FIG. **1A**, first of all, a support member **10** made up of a substrate (to be sometimes referred to as "dissimilar substrate" hereinafter) made of a material different from a nitride semiconductor and an underlayer **12** made of a nitride semiconductor formed on the substrate **11** is prepared.

In the specification and the claims, the "underlayer" means a layer made of a nitride semiconductor grown not by the growth method of the present invention but by a general nitride semiconductor growth method. This underlayer **12** may be of a single-layer structure or a multilayer structure. FIG. 1A shows the underlayer **12** as a buffer layer of a single-layer structure. Such a buffer layer eases or alleviates the lattice mismatch between the dissimilar substrate **11** and a nitride semiconductor crystal grown on the underlayer **12** to allow a nitride semiconductor crystal having better crystallinity to grow thereon. In general, this crystal is grown to several ten angstroms to several hundred angstroms at a low temperature less than 900° C., usually 500° C. to 800° C. It is especially preferable that such a low-temperature buffer layer be made of undoped GaN doped with no impurity. In the present invention, if the underlayer is formed to have a multilayer structure, a nitride semiconductor crystal having lesser crystal defects can be formed on the underlayer. In the present invention, for example, an underlayer of a multilayer structure can be made of a low-temperature buffer layer like the one described above, which is formed on the dissimilar substrate **11**, and another nitride semiconductor layer formed thereon. It is especially preferable that this another nitride semiconductor layer be made of $Al_xGa_{1-x}N$ ($0 \leqq x \leqq 0.5$). The another nitride semiconductor layer is formed to have a thickness larger than that of the low-temperature buffer layer, preferably 10 μm or less. The underlayer **12** can be grown by any of the known methods suitable for the growth of a nitride semiconductor, e.g., the metalorganic vapor-phase epitaxial method (MOVPE), the molecular beam epitaxial method (MBE), and the halide vapor-phase epitaxial growth method (HVPE), by using a gaseous Group 3 element source and a gaseous nitrogen source.

Referring to FIG. 1A again, a selective growth mask **13** having a plurality of windows **14***a* to **14***d* partly (selectively) exposing the underlayer **12** is formed on the underlayer **12** formed on the dissimilar substrate **11**. FIG. 1A shows, as a preferred form, the selective growth mask **13** as being made up of individual or discrete stripes **13***a* to **13***e* each having a rectangular cross-section. Referring to FIG. 1A, the spaces between the stripes **13** correspond to the windows **14***a* to **14***d*. The windows **14***a* to **14***d* will be sometimes generically referred to simply as a window **14** hereinafter.

As shown in FIG. 1B, nitride semiconductor portions **15** are grown from the surface portions, of the underlayer **12**, which are exposed from the windows **14***a* to **14***d* of the selective growth mask **13** by using a gaseous Group 3 element source and a gaseous nitrogen source according to the present invention. When nitride semiconductor portions are grown on the underlayer **12** whose surface is selectively covered with the selective growth mask **13** (or selectively exposed) in this manner, the nitride semiconductor portions do not grow on the entire surface of the selective growth mask **13** at first, but selectively grow on the portions, of the underlayer **12**, which are exposed by the windows **14**. When the nitride semiconductor portions further grow and exceed the upper end faces of the mask **13**, each nitride semiconductor crystal **15** exceeds a corresponding window **14** and then grows laterally on a corresponding selective growth mask **13**. Since the crystal defects in the underlayer **12** are covered with the selective growth mask **13**, the crystal defects are not easily dislocated to the portion, of the nitride semiconductor **15**, which grows laterally unlike a nitride semiconductor growing vertically like the underlayer **12**. In addition, the crystal defects of the underlayer **12** extend laterally as the nitride semiconductor crystal **15** grows on the selective growth mask **13**, but tends to stop halfway. Furthermore, some crystal defects dislocated through the window **14** appear on the upper surface of the nitride semiconductor layer, but the crystal defects tend to stop halfway.

When the nitride semiconductor portions for the nitride semiconductor crystals **15** keep growing in this manner, the adjacent nitride semiconductor crystals **15** that grow laterally and vertically on the selective growth mask **13** are joined to each other. Finally, as shown in FIG. 1C, all the crystals **15** combine into an integral nitride semiconductor crystal **16**. Narrow, small cavities **17***a* to **17***e*, each located in substantially the middle of the upper surface of a corresponding one of the stripe masks **13***a* to **13***e*, having a triangular cross-section, and extending in the longitudinal direction of each of the stripes **13***a* to **13***e*, prove that the adjacent nitride semiconductor crystals **15** grow laterally on the selective growth mask **13** and then grow vertically to combine with each other (in FIGS. 1A to 1C, the wavy lines and the bent lines on the underlayer **12**, the nitride semiconductor portions crystals **15**, and the nitride semiconductor crystal **16** indicate crystal defects (penetrating dislocations); the same applies to FIGS. 5A and 6A to 6C).

More specifically, relatively many crystal defects are generated in the underlayer **12** grown on the different type of substrate **11** or portions of the initially grown nitride semiconductor crystals **15** due to the lattice mismatch between the dissimilar substrate **11** and the nitride semiconductor portions. During the growth of the nitride semiconductor portions **15**, these crystal defects can be transferred to the leading or front surfaces of the grown crystals. The nitride semiconductor crystal **16** formed on the selective growth mask **13** is not grown from the substrate **11** or the underlayer **12** but is formed such that the nitride semiconductor crystals **15** grow laterally, and the adjacent nitride semiconductor crystals **15** finally combine with each other. Therefore, the number of crystal defects in the nitride semiconductor crystal **16** formed on the selective growth mask **13** is much smaller than that in the crystals directly grown from the dissimilar type of substrate **11** or the nitride semiconductor crystal portions initially grown from the underlayer **12** into the windows **14***a* to **14***f*. By using this combined nitride semiconductor crystal **16** as a growth substrate for various nitride semiconductor layers constituting a device structure, a nitride semiconductor device having crystallinity superior to that of a conventional device and hence having excellent performance can be realized.

The principle of a nitride semiconductor growth method according to the second aspect of the present invention will be described next with reference to FIGS. 1A to 1C. In the nitride semiconductor growth method according to the second aspect, a selective growth mask **13** is formed such that the total area of the upper surfaces of the portions, of a support member **10**, which are covered with the selective growth mask **13** is larger than the total area of the upper surfaces of the portions, of the support member **10**, which are exposed through windows **14***a* to **14***f*. A nitride semiconductor crystal **16** having fewer crystal defects can be obtained by setting the total area of the upper surfaces of the portions, of the support member **10**, which are covered with the selective growth mask **13** to be larger than the total area of the upper surfaces of the portions, of the support member **10**, which are exposed through windows **14**. In the second aspect, the combined nitride semiconductor crystal **16** can be grown by the same method as in the first aspect except for the use of the selective growth mask **13** having this relationship between the total area of the covered surfaces and the total area of the exposed surfaces (see the above description about the first aspect, made with respect to FIGS. 1A to 1C).

In the second aspect, an underlayer **12** is preferably present for the above reason described concerning the first aspect, but can be omitted. That is, in the specification and the claims, a support member can be made of only a dissimilar substrate **11**, or of the dissimilar substrate **11** and the underlayer **12** formed thereon.

Obviously, in the first aspect as well, the selective growth mask **13** is preferably formed such that the total area of the upper surfaces, of the support member **10**, which are covered with the selective growth mask **13** is larger than the total area of the upper surfaces, of the support member **10**, which are exposed through the windows **14***a* to **14***f*.

Preferable conditions for the nitride semiconductor growth method according to the present invention will be described next.

<Dissimilar Substrate>

As described above, the dissimilar substrate **11** is not specifically limited as long as it is made of a material different from a nitride semiconductor. For example, a substrate made of a material different from a nitride semiconductor such as an insulating substrate like a sapphire having the C plane ((0001) plane), the R plane ((1$\bar{1}$02) plane), or the A plane ((11$\bar{2}$0) plane) as a major surface or spinnel ($MgAl_2O_4$), an SiC (including 6H, 4H, and 3C), a ZnS substrate, a GaAs substrate, or an Si substrate, can be used. Note that an oxide substrate (e.g., a ZnO substrate or $La_xSr_{1-x}Al_yTa_{1-y}O_3$ substrate) that can ensure lattice match with a nitride semiconductor may be used, although it tends to decompose during the growth of the nitride semiconductor. The dissimilar substrate can have a major surface size of a diameter of 1 inch or 1 inch square or more, and preferably has a major surface size of a diameter of on 1 inch or 1 inch square to a diameter of 3 inches or 3 inches square. The nitride semiconductor crystal grown by the present invention can have a surface size almost equal to that of this dissimilar substrate.

As the dissimilar substrate **11**, a substrate having a major surface off-angled from the horizontal plane, preferably a major surface off-angled stepwise, can be used. Such a substrate will be described in detail with reference to, for example, FIG. **2** showing an enlarged view of a sapphire substrate **11** having a major surface off-angled stepwise. This substrate **11** has substantially horizontal terrace portions A and stepped portions B. The terrace portions A are regularly formed while the average size of uneven portions on the surface of each terrace portion A is adjusted to about 0.5 angstroms, and the maximum size is adjusted to about 2 angstroms. The size of each stepped portion B is preferably 30 angstroms or less, more preferably 25 angstroms or less, and most preferably 20 angstroms or less. The lower limit of the size of each stepped portion B is preferably 2 angstroms or more. Stepped portions each having such an off angle θ are preferably formed continuously on the entire surface of the dissimilar substrate **11**, but may be partly formed. As shown in FIG. **2**, the off angle θ of the major surface off-angled stepwise is the angle defined by a straight line connecting the bottom portions of a plurality of stepped portions and the horizontal plane of the terrace portion on the uppermost layer. When a sapphire substrate having a C plane as a major surface is used as the dissimilar substrate **11**, the off angle θ with respect to the C plane is 1° or less, preferably 0.8° or less, and more preferably 0.6° or less. With the use of a dissimilar substrate having a major surface off-angle in this manner, the interatomic distance between the nitride semiconductor to be grown according to the present invention and the dissimilar substrate decreases, thereby obtaining a nitride semiconductor substrate having few crystal defects.

<Selective Growth Mask>

The selective growth mask **13** does not substantially grow any nitride on its surface. This selective growth mask **13** is made of a material having the property of not growing any nitride semiconductor on its surface or making the growth of any nitride semiconductor on its surface difficult. For example, such a material includes oxides and nitrides such as silicon oxide (SiO_x), silicon nitride (Si_xN_y), titanium oxide (TiO_x), and zirconium oxide (ZrO_x), and multilayer films containing these components. In addition, metals having melting points of 1,200° C. or more (e.g., W, Ir, and Pt) can be used. These selective growth mask materials stand growth temperatures of about 600° C. to 1,100° C. that are set to grow nitride semiconductor portions according to the present invention, and has the property of inhibiting the growth of any nitride semiconductor on its surface or making the grow of any nitride semiconductor difficult. For example, a vapor-phase film forming technique such as vapor deposition, sputtering, or CVD can be used to form a selective growth mask on the upper surface of the support member **10**. In addition, the selective growth mask **13** having the windows **14** can be formed by using these materials as follows. A photomask having a predetermined shape is manufactured by photolithography. A film made of the above material is formed by a vapor-phase technique through this photomask, thereby forming the selective growth mask **13** having a predetermined shape. The shape of the selective growth mask **13** is not specifically limited. For example, this mask can be formed to have a dot pattern, a stripe pattern, or a lattice pattern. As will be described later, however, the selective growth mask is preferably formed as a plurality of individual or discrete stripes each oriented in a specific plane azimuth.

As described above, the selective growth mask **13** is preferably made up of a plurality of individual stripes **13***a* to **13***e*), as shown in FIG. **1**A. In this case, the width (Ws) of each stripe mask is preferably 0.5 to 100 μm, more preferably 1 to 50 μm, still more preferably 5 to 20 μm, and especially preferably 5 to 15 μm. The ratio (Ws/Ww) of the width to the interval between the respective stripe masks (corresponding to the width of each window (Ww)) is preferably 1 to 20, and more preferably 1 to 10. It is especially preferable that the width of each stripe mask be larger than the width of each window. In this case, the ratio Ws/Ww more preferably falls within the range of more than 1 and up to 20, and more preferably more than 1 and up to 10. When the interval (Ww) between the stripe masks is set to 8 μm or less, preferably 5 μm or less, and more preferably 3 μm or less, a nitride semiconductor crystal having a much smaller number of crystal defects can be grown. The interval (Ww) between the stripe masks is preferably 0.1 μm or more. The respective stripe masks preferably have substantially the same width and thickness and are preferably formed at substantially the same intervals on the entire surface of the support member **10** to be parallel to each other.

The thickness of the selective growth mask **13** is preferably 0.01 to 5 μm, more preferably 0.1 to 3 μm, and especially preferably 0.1 to 2 μm.

The selective growth mask **13** inhibits any nitride semiconductor from growing from the portions covered with the mask and allows nitride semiconductor portions to selectively grow from the portions exposed through the windows. Owing to this function, this mask is referred to as a "selective growth" mask in the specification and the claims.

<Preferable Relationship between Dissimilar Substrate and Selective Growth Mask>

FIG. **3** is a view of a unit cell showing the crystal structure of a nitride semiconductor. Strictly speaking, the nitride

semiconductor has a rhombic structure, but can be approximated to a hexagonal system in this manner. According to the method of the present invention, a sapphire substrate having the C plane as a major surface is preferably used as the dissimilar substrate **11**, and the selective growth mask **13** is preferably made up of a plurality of individual stripes extending parallel in a direction perpendicular to the sapphire A plane (in other words, extending parallel in a direction (the <1$\bar{1}$00> direction of the nitride semiconductor) parallel to the M plane (($1\bar{1}00$) plane) of the nitride semiconductor). That is, in FIG. **4**, which is a plane view of the sapphire substrate on the major surface side, the sapphire substrate **11** has the sapphire C plane as the major surface and an orientation flat (ORF) surface as the A plane. As shown in FIG. **4**, the selective growth mask **13** is preferably made up of a plurality of individual stripes extending parallel in a direction perpendicular to the sapphire A plane. It should be noted that although FIG. **4** shows only five individual stripes for the sake of easy understanding, more individual stripes are actually formed.

When a nitride semiconductor is to be selectively grown on the sapphire C plane, the nitride semiconductor tends to easily grow within the C plane in a direction parallel to the A plane, but does not easily grow in a direction perpendicular to the A plane. Therefore, the formation of stripe masks extending in a direction perpendicular to the A plane makes it easy to combine and grow the nitride semiconductor portions between the adjacent stripe masks on the respective stripe masks, thereby facilitating the growth of the nitride semiconductor crystal **16** shown in FIG. 1C. In this case, the leading surfaces, i.e., facets F (see FIG. **1B**), of the nitride semiconductor crystals **15** grown laterally on the mask **13** become the A planes of the nitride semiconductor portions.

Similarly, in the case wherein a sapphire substrate having an A plane as a major surface is used as well, if, for example, the ORF surface forms the R plane, the formation of a plurality of individual strip masks extending parallel in a direction perpendicular to the R plane makes it easy to grow nitride semiconductor portions in the direction of width of the stripe masks. This makes it possible to grow a nitride semiconductor crystal having few crystal defects.

The growth of nitride semiconductor portions exhibit anisotropy also with respect to spinnel ($MgAl_2O_4$). If the (111) plane is used as a growth surface (the major surface of the spinnel) for a nitride semiconductor, and the ORF surface forms the (110) plane, the nitride semiconductor tends to easily grow in a direction parallel to the (110) plane. If, therefore, a plurality of parallel, discrete strip masks are formed to extend in a direction perpendicular to the (110) plane, the adjacent nitride semiconductor crystals combine with each other on the selective growth mask **13**, thereby growing the nitride semiconductor crystal **16** having few crystal defects.

<Growth of Nitride Semiconductor Crystal>

The nitride semiconductor crystal to be grown according to the present invention can be grown by any of known methods suitable for the growth of a nitride semiconductor such as MOVPE, MBE, and HVPE, using a gaseous Group 3 element source and a gaseous nitrogen source. The nitride semiconductor crystal is preferably grown by MOVPE in the initial stage and grown by MOVPE or HVPE in the subsequent stage. As will be described in detail later, it is especially preferable that a nitride semiconductor crystal be grown by MOVPE in the initial stage and grown by HVPE in the subsequent stage.

When a nitride semiconductor is to be grown by MOVPE, the molar ratio of a nitrogen source gas to a Group 3 source gas (nitrogen source/Group 3 source molar ratio; to be sometimes referred to as a V/III ratio hereinafter) is preferably adjusted to 2,000 or less. The nitrogen source/Group 3 source molar ratio is preferably 1,800 or less, and more preferably 1,500 or less. The lower limit of the nitrogen source/Group 3 source molar ratio is not specifically limited as along as it is the stoichiometrical ratio or more. This lower limit molar ratio is preferably 10 or more, more preferably 30 or more, and most preferably 50 or more. If the molar ratio is higher than 2,000, triangular nitride semiconductor portions grow from the windows **14**. With this growth, crystal defects extend and scarcely stop halfway. As a result, the number of crystal defects increases. If the nitrogen source/ Group 3 source molar ratio is adjusted to 2,000 or less, the respective crystals **15** grow from the windows **14** first, and then grow laterally on the respective selective growth masks **13** while substantially maintaining their surfaces perpendicular to the upper surfaces of the selective growth masks. As a result, the similar perpendicular surfaces of the adjacent crystals that grow in the same manner come into contact and combine with each other on the selective growth mask **13**. For this reason, the crystal defects tend to stop halfway on the upper surface of the selective growth mask. In addition, the crystal defects extending from the windows **14** tend to stop halfway. Therefore, a nitride semiconductor crystal having a much smaller number of crystal defects can be grown. It is especially preferable that MOVPE be performed under a reduced pressure of 50 to 400 Torr.

In MOVPE, as a nitrogen source gas, for example, a hydride gas, such ammonia or hydrazine is used; as a Group 3 source gas, an organogallium gas, such as TMG (trimethylgallium) or TEG (triethylgallium), an organoaluminum gas, such as TMA (trimethylaluminum), or an organoindium gas such as TMI (trimethylindium) can be used.

When a nitride semiconductor, e.g., a gallium nitride crystal, is to be grown by HVPE, HCl gas is fed onto a molten gallium metal, and ammonia gas is fed from another gas feed pipe to combine these gases on the support member **10** to cause the following reaction:

$$GaCl+NH_3 \rightarrow GaN+HCl+H_2$$

In HVPE, since the growth rate of a nitride semiconductor crystal is several times higher than in MOVPE, for example, a 300-μm thick nitride semiconductor can be grown within several hours.

In the present invention, a nitride semiconductor crystal is preferably grown to a thickness of 1 μm or more, more preferably 5 μm or more, and most preferably 10 μm or more, although it depends on the width of each selective growth mask. These values correspond to the range of the lower limits of the thickness of a nitride semiconductor crystal, which is to be set to cover the upper portion of each selective growth mask. If this thickness is less than 1 μm, a growing nitride semiconductor crystal tends to be difficult to grow laterally on each selective growth mask. This tends to relatively increase the number of crystal defects. It is difficult to decrease the number of crystal defects under the condition in which nitride semiconductor portions are difficult to grow laterally. Although the upper limit of the thickness of the nitride semiconductor to be grown is not specifically limited, the thickness is preferably set to 70 μm or less when crystal growth is to be performed by MOVPE. If a nitride semiconductor crystal is grown to a thickness exceeding 70 μm, the growth time is prolonged, and the surface of the nitride semiconductor crystal becomes coarse. In addition, the selective growth masks tend to decompose. For these reasons, the above thickness is not preferable.

In the present invention, it is especially preferable that the nitride semiconductor crystal (e.g., the crystal **16** or a crystal **17**, **116**, or **76** to be described below) grown to provide a substrate for supporting a nitride semiconductor device be made of undoped gallium nitride or n-type impurity-doped gallium nitride.

To grow a thicker nitride semiconductor crystal with few defects, the nitride semiconductor crystal is preferably grown by MOVPE first, and then MOVPE is switched to HVPE to grow further nitride semiconductor crystal on the MOVPE crystal.

FIGS. **5**A and **5**B are sectional views for explaining a method of growing such a thicker nitride semiconductor crystal.

On the nitride semiconductor crystal **16**, which is grown by MOVPE according to the first or second aspect described with reference to FIGS. **1**A to **1**C, a nitride semiconductor **17** of the same type is grown to a thickness larger than that of the nitride semiconductor crystal **16**. When the nitride semiconductor **17** is grown on the MOVPE crystal **16** by HVPE, almost no crystal defects extend vertically. As a result, the crystal **17** having very few crystal defects can be grown as a whole. The crystal defects in the HVPE nitride semiconductor **17** are fewer than those in the MOVPE nitride semiconductor crystal **16** formed thereunder. Finally, for example, the nitride semiconductor crystal substrate **17** whose surface region has crystal defects of $1\times10^5/cm^2$ or less can be obtained. The crystal defects in the surface region are preferably $5\times10^4/cm^2$ or less, more preferably $1\times10^4/cm^2$ or less, and most preferably $1\times10^3/cm^2$ or less. Note that the "surface region" means a region having a depth of up to 5 μm from the upper surface (grown end face) of the nitride semiconductor crystal on the opposite side to the dissimilar substrate **11**. The number of crystal defects within 5 μm can be measured with a TEM (Transmission Electron Microscope). In the present invention, the crystal defects in a grown nitride semiconductor crystal are visually checked with a TEM (i.e., visual check on a TEM photograph) by two-dimensional observation, and indicate an average defect density (the same applies to the following Examples).

The HVPE nitride semiconductor crystal **17** is thicker than the MOVPE nitride semiconductor crystal **16**, and preferably has a thickness of 10 μm or more, more preferably 50 μm or more, and still more preferably 100 μm or more. If the thickness is less than 10 μm, the number of crystal defects tends to be difficult to decrease. Although the upper limit of thickness is not specified, the thickness is preferably 1 mm or less. If this crystal is grown to a thickness larger than 1 mm, the overall wafer warps due to the thermal expansion coefficient difference between the nitride semiconductor and the dissimilar substrate **11**. This tends to make it difficult to grow an HVPE nitride semiconductor crystal with uniform thickness.

In the present invention, when the nitride semiconductor crystal **16** and/or **17** is to be grown, the nitride semiconductor is preferably doped with an n-type impurity. In addition, the crystal **16** or **17** is preferably doped with this n-type impurity such that the n-type impurity concentration has a gradient in each crystal. The concentration gradient may be continuous or stepwise. It is especially preferable to set the concentration gradient of the n-type impurity in each of the crystals **16** and **17** such that the n-type impurity concentration decreases with an increase in distance from the dissimilar substrate **11**. In other words, the crystal **16** is preferably doped with the n-type impurity at higher concentrations with a decrease in distance from the dissimilar substrate **11**. Similarly, the crystal **17** is preferably doped with the n-type impurity at higher concentrations with a decrease in distance from the dissimilar substrate **11**. Assume that the n-type impurity concentration in each crystal decreases with a decrease in distance from the growth surface (major surface) in this manner. In this case, in forming an n-side electrode after a device structure is manufactured, when the nitride semiconductor substrate **16** is exposed by removing the dissimilar substrate **11**, the underlayer **12**, and the selective growth mask **13** or the nitride semiconductor substrate **17** is exposed by further removing the nitride semiconductor crystal substrate **16**, the surface region, of the nitride semiconductor crystal **16** or **17**, which is heavily doped with the n-type impurity can be exposed on the lower surface side. Therefore, by using this exposed surface as an n-side electrode formation surface, the output of the device can be increased by decreasing its Vf. In addition, even if etching is performed from the device structure side grown on the nitride semiconductor crystal substrate, and an electrode is formed on the etched surface, the nitride semiconductor crystal **16** or **17** heavily doped with the n-type impurity can be used as an n-electrode formation layer.

In the present invention, as the n-type impurity to be added to a nitride semiconductor crystal, a Group IV element, e.g., Si, Ge, Sn, or S, preferably Si and/or Sn, can be used. These n-type impurities can be added as hydrogenated substances or gaseous organic metallized substances during the growth of a nitride semiconductor. An n-type impurity is preferably added within the range of $5\times10^{16}/cm^3$ to $5\times10^{21}/cm^3$. If the impurity concentration is lower than $5\times10^{16}/cm^3$, since the carrier concentration of the nitride semiconductor crystal **16** or **17** becomes insufficient, the resistivity tends to increase. If the n-type impurity concentration is higher than $5\times10^{21}/cm^3$, the impurity concentration becomes excessively high. As a result, the crystallinity tends to deteriorate, and the number of crystal defects tends to increase. It is especially preferable to add an n-type impurity within the range of $1\times10^{17}/cm^3$ to $1\times10^{20}/cm^3$.

In the present invention, MOVPE can be switched to HVPE before the nitride semiconductor crystals **15** are combined into the integral crystal **16** by MOVPE (for example, in the state shown in FIG. **1**B). More specifically, although the nitride semiconductor crystals **15** have been grown laterally on the mask **13** by MOVPE, growth of the HVPE nitride semiconductor crystal **17** can be started before the adjacent nitride semiconductor crystals **15** combine with each other.

As shown in FIG. **5**A, after the nitride semiconductor crystals **16** and **17** are grown, the structure in FIG. **5**A can be used as a device substrate, and a desired nitride semiconductor device structure can be formed on the substrate. Alternatively, a nitride semiconductor substrate having a two-layer structure made up of the nitride semiconductor crystals **16** and **17** can be obtained by polishing/removing at least the dissimilar substrate **11**, the underlayer **12**, and the selective growth masks **13***a* to **13***e* of the structure shown in FIG. **5**A from the lower surface of the dissimilar substrate **11** in a direction perpendicular to the major surface of the dissimilar substrate **11**. If the nitride semiconductor crystal **16** is further removed, a free nitride semiconductor crystal substrate made of the HVPE nitride semiconductor crystal **17** can be obtained, as shown in FIG. **5**B. As is also apparent from the above description, this HVPE nitride semiconductor substrate is characterized in that the crystal defects in the surface region are $1\times10^5/cm^2$ or less. This substrate can have at least one of the following characteristics: that the substrate is doped with an n-type impurity; that this n-type impurity has a concentration gradient in the nitride semi-

conductor substrate; and that the n-type impurity concentration decreases with a decrease in distance from the major surface (grown end face) of the substrate (i.e., with an increase in distance from the dissimilar substrate **11**). From another viewpoint, the substrate obtained in this manner can be characterized in that it has first and second major surfaces, and is doped with an n-type impurity, and the n-type impurity has a concentration gradient in the substrate.

In the present invention, a buffer layer made of a nitride semiconductor can be grown first before the substantial portion of a nitride semiconductor crystal (e.g., a crystal to be grown laterally on each mask, such as the nitride semiconductor crystal **16**) is grown. This buffer layer can be made of a nitride semiconductor such as AlN, GaN, AlGaN, or InGaN, and can be grown to a thickness of several ten angstroms to several hundred angstroms at a low temperature less than 900° C. The scope of the present invention incorporates the growth of this low-temperature buffer layer after the growth of the substantial portion of the nitride semiconductor crystal. This buffer layer is formed to ease the lattice mismatch between the dissimilar substrate and the nitride semiconductor grown afterward, but can be omitted depending on the nitride semiconductor growth method, the type of substrate, and the like.

The second method of manufacturing a nitride semiconductor crystal having a smaller number of crystal defects will be described next with reference to FIGS. **6**A to **6**C. First of all, as shown in FIG. **6**A, after the surface of the nitride semiconductor crystal **16** grown according to the first or second aspect of the present invention, which has been described in detail above, is polished to provide a flat surface, a selective growth mask **113** having a plurality of windows for partly exposing the surface of the nitride semiconductor crystal **16** is formed on the surface of the nitride semiconductor crystal **16**. The description about the first selective growth mask **13** (the material, the shape, the width, the thickness, the shape of each window, the relationship with the dissimilar substrate, and the like) equally applies to the selective growth mask **113** unless otherwise specified.

The selective growth mask **113** is generally formed at a position shifted from the position where the first selective growth mask **13** is formed. That is, the selective growth mask **113** is formed to cover the surface of the portions, of the nitride semiconductor crystal **16**, on which the crystal defects produced from the interface between the support member **10** and the nitride semiconductor crystal **16** and extending from the windows **14***a* to **14***f* of the first selective growth mask **13**, thereby selectively exposing the surface of the nitride semiconductor crystal **16**. More specifically, in FIG. **6**A, similar to the first selective growth mask **13**, the selective growth mask **113** is made up of individual stripes **113***a* to **113***f*, and the respective stripes are positioned to cover the surface regions, of the nitride semiconductor crystal **16**, which correspond to the windows **14***a* to **14***f* of the selective growth mask **13**. The windows **114***a* to **114***e* are positioned in the regions corresponding to the substantially middle portions of the first strip masks **13***a* to **13***e*. By forming the selective growth mask **113** at the position corresponding to each window **14** of the first selective growth mask **13** in this manner, the selective growth mask **113** can prevent the crystal defects in the crystal **16** from penetrating.

The total surface area of the selective growth mask **113** (the portions, of the nitride semiconductor crystal **16**, which are covered with the mask) is preferably larger than the total surface area of the windows **14***a* to **14***f* of the selective growth mask **13** (the exposed portions, of the nitride semiconductor crystal **16**, which are exposed through the windows). More specifically, if the selective growth mask **113** is formed to have a dot pattern, a stripe pattern, or the like, the area of the surface of a unit dot is set to be larger than that of a unit stripe window. With this setting, a nitride semiconductor having less crystal defects can be grown on the crystal **16**.

When a nitride semiconductor crystal of the same type as that of the nitride semiconductor crystal **16** (preferably undoped or n-type impurity-doped GaN) is grown by the same method as that used to grow the nitride semiconductor crystal **16**, nitride semiconductor crystals **115** grow in the same manner as that described about the crystal **15** with reference to FIG. **1**B. Finally, the adjacent nitride semiconductor crystals **115** combine into the integral nitride semiconductor crystal **116**. In this case, the second nitride semiconductor crystals **115** grown on the first nitride semiconductor crystal **16** are the same type of nitride semiconductor portions as that of the nitride semiconductor crystal **16**. In addition, these crystals **115** are grown on the first nitride semiconductor crystal **16** having few crystal defects. For these reasons, crystal defects due to lattice mismatch do not easily occur, and fewer crystal defects are dislocated. Therefore, the second nitride semiconductor crystal **116** having excellent crystallinity can be obtained. By using this second nitride semiconductor crystal **116** as a growth substrate for a device structure, a nitride semiconductor device having excellent crystallinity can be realized. Obviously, the nitride semiconductor **116** can be doped with an n-type impurity as in the case of the nitride semiconductor **16** or **17** (see FIGS. **1**C and **5**A).

The growth of the second selective growth mask described with reference to FIGS. **6**A to **6**C and the subsequent growth of the nitride semiconductor crystal can be repeatedly performed. That is, if some portion of a nitride semiconductor crystal has lattice defects, a new mask can be formed on that portion, and a new nitride semiconductor can be grown on the mask.

The principle of a nitride semiconductor growth method according to the third aspect of the present invention will be described next. The third aspect of the present invention is associated with a nitride semiconductor growth method characterized in that after a nitride semiconductor is grown on a support member according to the present invention, a new nitride semiconductor is grown from this nitride semiconductor as a seed crystal in substantially only the lateral direction while the growth in the vertical direction is suppressed, and is grown in both the vertical and lateral directions afterward. In the present invention, to suppress the growth of the nitride semiconductor in the vertical direction is to prevent at least the nitride semiconductor from growing in the vertical direction. The nitride semiconductor can be grown in the lateral direction by exposing the surface of the initially grown nitride semiconductor in the vertical direction, and growing the above new nitride semiconductor from only the exposed surface. The nitride semiconductor whose growth direction is controlled in this manner starts to grow from the vertical direction to the lateral direction. As the growth continues, the nitride semiconductor starts to grow in the vertical direction again as well as in the lateral direction. In this manner, a nitride semiconductor crystal having a smaller number of crystal defects can be obtained.

The especially preferred embodiment of the nitride semiconductor growth method according to the third aspect of the present invention, in which the growth direction of a

nitride semiconductor is controlled in this manner, will be described in detail below with reference to the FIGS. 7A to 7D.

As shown in FIG. 7A, a nitride semiconductor layer **71** is preferably formed on almost the entire surface of a support member **10** made of a dissimilar substrate **11** on which an underlayer **12** is formed or not formed. The support member **10**, including the dissimilar substrate **11** and the underlayer **12**, is identical to the one sufficiently described above.

The nitride semiconductor layer **71** is preferably made of gallium nitride (GaN) doped with no impurity (undoped) or GaN doped with an n-type impurity like the one described above. The nitride semiconductor layer **71** can be grown on the support member **10** at a high temperature, specifically 900° C. to 1,100° C., and more preferably 950° C. to 1,050° C. The thickness of each portion, of the nitride semiconductor layer **71**, which is exposed from a side surface of a corresponding recess portion (to be described in detail later) after the formation of a growth control mask (to be described in detail later) is not specifically limited. However, the nitride semiconductor layer **71** is preferably formed such that each portion exposed from a side surface of a corresponding recess portion has a thickness of 100 angstroms or more, preferably about 1 to 10 μm, and more preferably about 1 to 5 μm.

As shown in FIG. 7B, a plurality of recess portions (FIG. 7B shows six recess portions **72***a* to **72***f*; these recess portions will be sometimes generically referred to as recess portions **72** hereinafter) are formed in the nitride semiconductor layer **71** formed on the support member **10**, and the first nitride semiconductor layer **71** is selectively exposed on the side surfaces of the respective recess portions **72**. Thereafter, first growth control masks **73***a* to **73***g* and second masks **74***a* to **74***f* are formed on the upper surface portions of the nitride semiconductor layer **71** and the bottom surfaces of the recess portions **72***a* to **72***f*. The first growth control masks **73***a* to **73***g* will be sometimes generically referred to as first growth control masks or masks **73** hereinafter. The second growth control masks **74***a* to **74***f* will be sometimes generically referred to as second growth control masks or masks **74** hereinafter. The first and second growth control masks **73** and **74** can be formed by using the same material as that for the selective growth masks described above and the same method as used therefor.

The plurality of recess portions **72***a* to **72***f* may have any shapes as long as they allow the nitride semiconductor layer **71** to be selectively exposed on their side surfaces. For example, each recess portion can be formed into a cylindrical shape, a prismatic shape, or a groove-like shape. It is preferable that the bottom surface of each recess portion **72** be substantially parallel to the upper surface of the support member **10**.

Each recess portion **72** formed in the nitride semiconductor layer **71** reaches some midpoint in the nitride semiconductor layer **71**, the surface of the support member **10**, or a portion in the support member **10**. Although the depth of each recess portion **72** is influenced by the thickness of the nitride semiconductor layer **71**, the thickness of each second growth control mask **74**, and the like, it suffices to set the depth of each recess portion **72** such that the second growth control mask **74** formed on the bottom surface of the recess portion **72** prevents the dissimilar substrate **11** from being exposed, and the second growth control masks **74** is formed to have a sufficient thickness so as not to interfere with the growth of a new nitride semiconductor grown laterally from that surface, of the nitride semiconductor layer **71**, which is exposed from a side surface of the recess portion **72**. Each recess portion **72** is preferably formed at a depth that does not expose the substrate **11**, and it is especially preferable that each recess portion **72** be formed at a depth corresponding to some midpoint in the direction of thickness of the nitride semiconductor layer **71**. If the recess portion **72** is formed at a depth at which the dissimilar substrate **11** is exposed through the bottom surface of the recess portion **72**, it is difficult to form the second growth control masks **74** near the corners of the bottom surface of the recess portion **72**. If the second growth control masks **74** do not sufficiently cover the surface portions of the dissimilar substrate **11**, new nitride semiconductor portions may grow from the dissimilar substrate **11**, resulting in crystal defects. Although the depths of the recess portions **72** may differ from each other, the recess portions **72** are generally formed to have the same depth.

To form the recess portions **72**, any method capable of partly removing the nitride semiconductor layer **71** can be used. Such a method includes etching, dicing, and the like. According to dicing, recess portions **72** made of parallel grooves each having a rectangular cross-section or recess portions **72** made of lattice grooves can be easily formed.

When the recess portions **72** are selectively formed in the nitride semiconductor layer **71** by etching, a striped photomask, a lattice photomask, and the like are manufactured by using mask patterns in various forms in photolithography, and a resist pattern is formed on the nitride semiconductor layer **71**, thereby etching the nitride semiconductor layer **71**. Methods of etching the nitride semiconductor layer **71** include wet etching, dry etching, and the like. To form smooth surfaces, dry etching is preferably used. Dry etching includes reactive ion etching (RIE), reactive ion beam etching (RIBE), electron cyclotron etching (ECR), ion beam etching (IBE), and the like. In any of these methods, the desired recess portions **72** can be formed by etching the nitride semiconductor by appropriately selecting an etching gas. For example, the etching means for a nitride semiconductor disclosed in Jpn. Pat. Appln. KOKAI Publication No. 8-17803 previously filed by the present applicant can be used.

When the recess portions **72** are to be formed by etching, each side surface of each recess portion **72** may be almost vertical to the dissimilar substrate **11** as shown in FIG. 7B, or may have a mesa shape or inverted mesa shape.

The first and second masks **73** and **74** can be formed in slightly different manners depending on whether the recess portions **72** are formed by etching or dicing.

When the recess portions **72** are to be formed by etching, a layer made of a mask material is formed first on the first nitride semiconductor layer **71**, and then a resist film is formed on the layer. After a predetermined pattern is transferred, exposed, and developed to form the first mask **73**, the nitride semiconductor layer **71** is etched to form the recess portions **72**. Subsequently, a growth control mask material layer is formed on the nitride semiconductor layer **71** in which the recess portions **72** are formed, i.e., the masks **73**, the bottom and side surfaces of the recess portions **72**, and the like, and the mask material layer on the side surfaces of the recess portions **72** is selectively etched to form the second masks **74** by dry etching using, for example, CF_4 gas and O_2 gas. With this formation, although FIG. 7B shows the first mask **73** as a single layer, the first mask **73** has two-layer structure in which the mask material layer is further formed on the first mask **73**. Obviously, the first and second masks **73** and **74** may be formed on the portions where the first masks **73** are formed and the bottom surfaces of the recess portions **72** by the same method as described above after the first masks **73** are removed before the second masks **74** are formed.

When the recess portions **72** are to be formed by dicing, the recess portions **72** are formed by removing the nitride semiconductor layer **71** from the upper surface with a dicing saw, and a growth control mask material layer is formed on the entire surface of the nitride semiconductor layer **71**, including the recess portions **72**, as described above. Thereafter, only the growth control mask material layer on the side surface portions of the recess portions **72** is etched by dry etching using CF_4 gas and O_2 gas, thereby simultaneously forming the first and second growth control masks **73** and **74**.

The first and second growth control masks **73** and **74** may be formed to have the same thickness as long as they have thicknesses that do not interfere with the growth of a nitride semiconductor crystal to be described in detail later. For example, when the underlayer **12** is not formed on the dissimilar substrate **11**, the second growth control masks **74** are preferably formed to have a sufficient thickness so as not to expose the dissimilar substrate **11** to the bottom surfaces of the recess portions **72**, and preferably a sufficient thickness that inhibits formation of pinholes in the dissimilar substrate **11** due to the influence of heat. Obviously, however, the masks **74** must not be thickened to such an extent as to interfere with the growth of nitride semiconductor crystals from the portions, of the nitride semiconductor layer **71**, which are exposed to the side surfaces of the recess portions. If pinholes are formed in the second masks **74**, nitride semiconductor portions may grow through the pinholes. This is considered as a cause for crystal defects. If, for example, the first growth control mask **73** is formed to be relatively thin, the barrier height that a nitride semiconductor crosses (the thickness of the first growth control mask **73**) decreases. Therefore, a nitride semiconductor easily grows laterally on the masks **73**. The formation of such growth control masks is obvious to a person skilled in the art. For example, these growth control masks can be formed in two separate processes.

The relationship between the first growth control mask **73** and the dissimilar substrate **11** is preferably equivalent to the previously described relationship between the selective growth mask and the dissimilar substrate **11**. Therefore, the items described under the title <Preferable Relationship between Dissimilar Substrate and Selective Growth Mask> equally apply to the first growth control mask **73**. More specifically, the first growth control mask **73** is preferably made up of a plurality of individual stripes each having a substantially rectangular cross-section. In this case, the respective individual stripes are preferably formed on the sapphire C plane to extend parallel in a direction perpendicular to the sapphire C plane, or on the sapphire A plane to extend parallel in a direction perpendicular to the sapphire R plane. Alternatively, the respective individual stripes are preferably formed on the spinnel (111) plane to extend parallel in a direction perpendicular to the spinnel (110) plane. Therefore, the respective recess portions **72** are preferably formed by a plurality of individual grooves extending in the same direction as that of the striped growth control mask **73**. The top surface of each wall defined between adjacent grooves preferably has the same plane shape as that of each striped growth control mask **73**.

Each of the plurality of striped growth control masks **73** preferably has a width (corresponding to the width Ws of the first selective growth mask) of 1 to 20 μm, and more preferably 10 to 20 μm. The interval between the masks **73** is preferably 1 to 20 μm, and more preferably 2 to 5 μm.

After the recess portions **72** and the first and second growth control masks **73** and **74** are formed in this manner, nitride semiconductor portions **75** are grown from the exposed side surfaces of the nitride semiconductor layer **71** by the vapor-phase growth method described in association with the first and second aspects, as shown in FIG. 7C.

As described with reference to FIG. 7B, the upper surface portions (i.e., the top surfaces of the walls between the recess portions) of the nitride semiconductor layer **71**, except for the side surfaces of the recess portions **72** formed therein, and the bottom surfaces of the recess portions **72** are covered with the growth control masks **73** and **74**, and the nitride semiconductor layer **71** is exposed on only the side surfaces of the recess portions **72**. For this reason, ;nitride semiconductor portions are grown from only these selective exposed surfaces of the nitride semiconductor layer **71** by the vapor-phase growth method. That is, the nitride semiconductor portions **75** start to grow laterally from the exposed side surfaces of the nitride semiconductor layer **71**. As the nitride semiconductor portions **75** keep growing, they start to grow vertically as well as laterally. When the nitride semiconductor portions **75** reach the upper surfaces of the recess portions **72**, each nitride semiconductor portion grows laterally from the two sides of each recess portion on the first growth control mask **73**. Ams described in association with the first and second aspects, the adjacent nitride semiconductor portions **75** combine into an integral nitride semiconductor crystal **76**, as shown in FIG. 7D. The nitride semiconductor crystal **73** whose growth direction is controlled in the initial growth period has good crystallinity with very few crystal defects even if the crystal is grown thick.

The nitride semiconductor crystal **75** to be grown is preferably a nitride semiconductor of the same type as that of the nitride semiconductor layer **71**, and especially preferably undoped or n-type impurity-doped GaN. When the nitride semiconductor crystal **76** is to be doped with an n-type impurity during growth, the impurity can have a concentration gradient, as described previously.

In the third aspect, the second growth control mask **74** is preferably formed. Even if this mask is not; formed, a nitride semiconductor crystal having excellent crystallinity can be grown. In this case, the description about the first selective growth masks **13** and the first windows **14** in association with the first and second aspects can be equally applied to the first growth control masks **73** and the recess portions **72** by regarding the first selective growth masks **13** and the first windows **14** described in association with the first and second aspects as the first growth control masks **73** and the recess portions **72**. In this case, each recess portion **72** should have a depth that does not expose the surface of the support member **10**. In this case, it is especially preferable that each recess portion have a depth of 500 angstroms to 5 μm.

As is obvious from the above description, each of the nitride semiconductor crystals **16**, **17**, **116**, and **76** (to be sometimes generically referred to as a substrate **1000** hereinafter) grown by the method of the present invention has very few defects, and can be effectively used as a substrates for supporting a predetermined nitride semiconductor device thereon.

It can be described that a nitride semiconductor substrate of the present invention, especially the nitride semiconductor substrate grown by the method according to the first to third aspects, has first and second major surfaces, the crystal defects in a region near the first major surface (i.e., the surface on which a device structure is supported or the grown end face) are relatively few, and the crystal defects in a region near the second major surface are relatively many.

The second major surface is a major surface closer to the dissimilar substrate **11** than the first major surface. If this nitride semiconductor substrate is doped with an n-type impurity, since the n-type impurity tends to concentrate in a region having many crystal defects, a surface region near the second major surface can form an n+-type region. If, therefore, an n-side electrode of a nitride semiconductor device is formed in this region, the threshold or forward voltage of the device can be decreased.

It can also be described that regions (first regions) each having a relatively small number of crystal defects and regions (second regions) each having a relatively large number of crystal defects are unevenly distributed when viewed from the first major surface of the nitride semiconductor substrate of the present invention. The first regions correspond to the masks **13** and **73**. The second regions correspond to the windows **14** and the recess portions **72**.

The device structure of the nitride semiconductor device of the present invention is supported on the nitride semiconductor substrate of the present invention. In this case, the nitride semiconductor substrate of the present invention may support the device structure in a free state wherein the support member **10** and the masks (**13**, **113**, **73**, **74**, or the like) are removed, or may support the device structure in a state wherein the support member **10** and the masks are formed. In addition, the device structure can be formed on the nitride semiconductor of the present invention in the free state set in advance, or the nitride semiconductor can be set in the free state by removing the support member **10** and the masks after the device structure is formed on the nitride semiconductor with the support member **10** and the masks being formed.

The nitride semiconductor substrate in the free state according to the present invention preferably has a thickness of 70 μm or more, more preferably 100 μm or more, and still more preferably 300 μm or more. With a thickness of 70 μm or more, the nitride semiconductor substrate becomes resistant to cracking and allows easy handling. Although the upper limit of the thickness is not specified, the substrate preferably has a thickness of 1 mm or less.

The nitride semiconductor substrate having the dissimilar substrate according to the present invention preferably has a thickness of 1 to 50 μm. If the thickness falls within this range, the frequency of warpage of the overall wafer due to the thermal coefficient difference between the nitride semiconductor substrate and the dissimilar substrate **11** decreases.

The device structure to be supported on the nitride semiconductor substrate of the present invention is not specifically limited as long as it has a predetermined device function, and includes an LED device structure, an LD device structure, and the like. However, the device structure is not limited to these. The device structure of the present invention can include at least an n- or p-type nitride semiconductor. For example, a device structure can be presented, which has an n-type nitride semiconductor layer having a superlattice structure as an n-type nitride semiconductor layer, and in which an n-type nitride semiconductor that allows an n-side electrode to be formed on the n-type layer of this superlattice structure is formed. For example, each of the LED device and LD device of the present invention basically has an active layer and two cladding layers formed on the two sides of the active layer.

In addition, as other arrangements of the nitride semiconductor device, e.g., electrode and device shapes, any suitable electrode and shape can be used.

In the present invention, the p and n sides mean opposite sides with respect to, for example, an active layer; the p side is a side including a nitride semiconductor layer that can be doped with a p-type impurity, and the n side is a side including a nitride semiconductor layer that can be doped with an n-type impurity.

FIG. **8**A is a schematic sectional view showing the LED device structure formed on the nitride semiconductor substrate **1000**. FIG. **8**B is a plan view of the structure. As is apparent from FIG. **8**B, this LED device has an almost rectangular parallelepiped shape as a whole.

As shown in FIG. **8**A, an n-side buffer layer **81** made of a nitride semiconductor doped with an n-type impurity such as Si, e.g., n-type GaN, is formed on the nitride semiconductor substrate **1000**. In general, this buffer layer **81** is a nitride semiconductor crystal grown at a high temperature of 900° C. or more. This high-temperature buffer layer **81** is discriminated from a low-temperature buffer layer (e.g., the buffer layer **12** in FIGS. **1**A to **1**C) to be grown at a low temperature to ease the lattice mismatch between the substrate and the nitride semiconductor grown thereon, and serves as an n-type cladding layer. In manufacturing an LED device, the buffer layer **81** is preferably formed to have a thickness of 20 angstroms or more. The buffer layer **81** preferably has a distorted superlattice structure formed by alternately stacking first and second nitride semiconductor layers having different compositions. The buffer layer having the superlattice structure can provide an n-side cladding layer having excellent crystallinity as a carrier confining layer. For example, a buffer layer having such a superlattice structure can be formed by alternately stacking an aluminum-containing nitride semiconductor doped with an n-type impurity, especially thin AlGaN layers, and undoped GaN layers. Note that the buffer layer having the superlattice structure preferably has a thickness of 50 angstroms or more.

An active layer **82** is formed on the buffer layer **81**. It is especially preferable that the active layer **82** have a quantum well structure including a well layer made of InGaN. The quantum well structure includes both a single quantum well (SQW) structure and a multi quantum well (MQW) structure. The multi quantum well structure is preferable. An active layer having a multi quantum well structure can be formed by, for example, alternately stacking first and second thin InGaN layers having different compositions or alternately stacking thin InGaN layers and GaN layers. When the active layer **82** has a quantum well structure, one or both of the well layer and the barrier layer can be doped with an n- or p-type impurity or no impurity. If the active layer **82** has not a quantum well structure, the active layer is doped with an n-type impurity and/or a p-type impurity.

A p-side cladding layer **83** made of a p-type nitride semiconductor doped with a p-type impurity, e.g., Mg, is formed on the active layer **82**. The p-side cladding layer **83** is preferably made of an aluminum-containing nitride semiconductor, especially AlGaN.

A p-side contact layer **84** made of a p-type nitride semiconductor doped with a p-type impurity, e.g., Mg, is formed on the p-side cladding layer **83**. It is especially preferable that this p-side contact layer **84** be made of p-type GaN.

A light-transmitting p-electrode **85** is formed on almost the entire surface of the p-side contact layer, and a disk-like bonding pad **86** is formed on substantially the central portion of the p-electrode **85**.

As shown in FIG. **8**A, the p-side contact layer **84**, the p-side cladding layer **83**, the active layer **82**, and the buffer layer **81** are etched to expose their side surfaces. This etching proceeds until it reaches a portion in the surface of the substrate **1000** to form a "cutting margin". The formation of the cutting margin upon etching in this manner reduces

the impact applied to the p-n junction when each chip is cut later. As a result, LED devices each having higher reliability can be obtained, and the yield improves. In addition, this "cutting margin" is preferably formed on a portion corresponding to each window portion **14** of the first selective growth mask **13**. Furthermore, with the formation of the "cutting margin", when the sapphire substrate, the first selective mask, and the like are removed, a chip cutting position that indicates a region having many crystal defects and a region having few crystal defects can be accurately discriminated.

As described above, by doping the nitride semiconductor substrate **1000** with an n-type impurity, an n-side electrode **87** can be formed on the entire lower surface of the substrate **1000**.

FIG. **9** schematically shows a cross-section of an LED device having a structure similar to that of the LED device in FIGS. **8**A and **8**B except that the nitride semiconductor substrate of the present invention is kept supported on the support member **10**. In the LED device shown in FIG. **9**, a p-side contact layer **84**, a p-side cladding layer **83**, and an active layer **85** are etched to expose their side surfaces. This etching reaches the n-side buffer layer **81** as well to partly leave the n-side buffer layer **81**. An n-side electrode **87** is formed on the surface of the left n-side buffer layer **81**.

FIG. **10** is a schematic sectional view showing the laser diode (LD) structure formed on the substrate **1000** of the present invention.

A buffer layer **111** made of a nitride semiconductor is formed on the nitride semiconductor substrate **1000**. This buffer layer **211** is a nitride semiconductor single-crystal layer grown at a high temperature of 900° C. or more. This layer is discriminated from a low-temperature buffer layer (e.g., the buffer layer **12** in FIGS. **1**A to 1C) to be grown at a low temperature to ease the lattice mismatch between the substrate and the nitride semiconductor grown thereon. When an LD device is to be manufactured, this buffer layer **211** preferably has a thickness of 100 angstroms or less, more preferably 70 angstroms or less, and most preferably 50 angstroms or less, and is preferably formed into a distorted superlattice structure obtained by alternately stacking first and second thin nitride semiconductor layers having different compositions. With the distorted superlattice structure, the crystallinity improves, and hence a high-output LD device can be realized. Note that this buffer layer **211** can be omitted.

A crack prevention layer **212** made of a nitride semiconductor is formed on the buffer layer **211**. If this crack prevention layer **212** is made of an indium-containing n-type nitride semiconductor, preferably InGaN, the occurrence of cracks in the aluminum-containing nitride semiconductor layer that can be formed layer can be effectively prevented. The crack prevention layer **212** is most preferably made of $In_xGa1-xN$ ($0<x<0.5$). The crack prevention layer **212** is preferably formed to have a thickness from 100 angstroms to 0.5 μm. If this layer is thinner than 100 angstroms, the layer is difficult to serve as a crack prevention layer. If the layer is thicker than 0.5 μm, the crystal itself tends to become black. Note that the crack prevention layer **212** can be omitted.

An n-side cladding layer **213** made of an n-type nitride semiconductor is formed on the crack prevention layer **212**. This n-side cladding layer **213** serves as both a carrier confining layer and a light confining layer. The n-side cladding layer **213** preferably has a superlattice structure obtained by alternately stacking first and second nitride semiconductor portions having different band gap energies. Such a superlattice structure preferably includes an aluminum-containing nitride semiconductor, and more preferably AlGaN. In this case, the threshold of the LD device can be decreased by performing so-called modulated doping, i.e., doping either the first layer or the second layer with an impurity at a higher concentration. For example, the n-side cladding layer **213** having such a superlattice structure can be formed by alternately stacking thin AlGaN layers doped with an n-type impurity, e.g., Si, and undoped thin GaN layers. The superlattice structure can provide a carrier confining layer having good crystallinity without any crack. The n-side cladding layer **213** preferably has a thickness from 100 angstroms to 2 μm, and more preferably from 500 angstroms to 1 μm.

An n-side light guide layer **214** made of a nitride semiconductor is formed on the n-side cladding layer **213**. This n-side light guide layer **214** serves as a guide layer for light from an active layer **215** (to be described later), and is preferably made of GaN or InGaN. The n-side light guide layer **214** is preferably formed to have a thickness of 100 angstroms to 5 μm, and more preferably 200 angstroms to 1 μm. In general, the n-side light guide layer **214** is doped with an n-type impurity, e.g., Si or Ge, to have an n-type conductivity, but not be doped with such an impurity. The n-side light guide layer **214** can be a layer having a superlattice structure. The n-side light guide layer **214** having such a superlattice structure can be formed by alternately stacking, for example, first layers made of a first nitride semiconductor, e.g., GaN, and second layers made of a second nitride semiconductor different from the first nitride semiconductor, e.g., InGaN. In this case, at least one of the first and second layers may be doped with an n-type impurity or may not be doped.

In the present invention, the magnitude of band gap energy is determined with reference to the band gap energy of a layer having a higher band gap energy in a superlattice structure, whereas the magnitude of band gap energy of an active layer having a quantum well structure is determined with reference to the band gap energy of a well layer.

The active layer **215** made of a nitride semiconductor is formed on the n-side light guide layer **214**. It is especially preferable that this active layer **215** have a quantum well structure having a well layer made of an indium-containing nitride semiconductor (preferably InGaN or InAlN). Such a quantum well structure may be a single quantum well (SQW) structure or a multi quantum well (MQW) structure including a well layer and a barrier layer. The multi quantum well structure is preferable. For example, a multi quantum well structure can be formed by alternately stacking InGaN nitride semiconductors having different compositions, or may be formed by alternately stacking GaN and InGaN layers. An active layer having a quantum well structure allows a well layer and/or a barrier layer to be doped with an impurity or no impurity. An active layer having an undoped quantum well structure is preferable. In this case, as a well layer, an InAlN layer can be used in place of an InGaN layer.

A p-side cap layer **216** having a band gap energy higher than that of a p-side light guide layer **217** (to be described later) and that of an active layer **215** (a well layer in a quantum well structure) is formed on the active layer **215**. The p-side cap layer **216** is preferably formed to have a thickness of 0.1 μm or less, more preferably 500 angstroms or less, and most preferably 300 angstroms or less. If the thickness of the p-side cap layer **216** is larger than 0.1 μm, the p-side cap layer **216** tends to crack. The p-side cap layer **216** therefore tends to be difficult to grow as Et nitride

semiconductor with good crystallinity. The p-side cap layer **216** is made of an aluminum-containing nitride semiconductor, especially preferably AlGaN in this case, as the composition ratio of Al of AlGaN increases, the laser oscillation of the LD device is facilitated with a decrease in the thickness of the p-side cap layer **216**. If, for example, the p-side cap layer **216** is to be made of $Al_yGa_{1-y}N$ wherein the y value is 0.2 or more, it is especially preferable to adjust the thickness of the p-side cap layer **216** to 500 angstroms or less. Although the lower limit of the thickness of the p-side cap layer **216** is not specified, the p-side cap layer **216** is preferably formed to have a thickness of 10 angstroms or more. The p-side cap layer **216** may be doped with a p-type impurity to become a p-type layer. However, this layer may be doped with an n-type impurity to become a carrier-compensated i-type layer or may be undoped because it is thin. Most preferably, the p-side cap layer **216** is doped with a p-type impurity.

The p-side light guide layer **217** made of a nitride semiconductor having a band gap energy lower than that of the p-side cap layer **216** is formed on the p-side cap layer **216**. This p-side light guide layer **217** serves as a guide layer for light from the active layer **215**, and is preferably made of GaN or InGaN, similar to the n-side light guide layer **214**. In addition, the p-side light guide layer **217** can serve as a barrier layer during the growth of a p-side cladding layer **218** (to be described later). The p-side light guide layer **217** is preferably formed to have a thickness of 100 angstroms to 5 μm, and more preferably 200 angstroms to 1 gm so as to serve as a desirable light guide layer. In general, the p-side light guide layer **217** is doped with a p-type impurity, e.g., Mg, to have a p-type conductivity, but may not be doped. Note that the p-side light guide layer **217** may have a superlattice structure. Such a superlattice structure can be formed by sequentially stacking first and second nitride semiconductor layers having different band gap energies. The p-side light guide layer **217** having this superlattice structure can be formed by alternately stacking, for example, first layers made of GaN and second layers made of InGaN. In this case, at least one of the first and second layers may be doped with a p-type impurity or may not be doped.

The p-side cladding layer **218** made of a nitride semiconductor is formed on the p-side light guide layer **217**. Similar to the n-side cladding layer **213**, this layer **218** serves as a carrier confining layer and a light confining layer. The p-side cladding layer **218** preferably contains an aluminum-containing nitride semiconductor, and more preferably AlGaN. When this layer is formed as a superlattice structure, it serves to decrease the resistivity of the p-side layer. Such a superlattice structure can be formed by sequentially stacking first and second nitride semiconductor layers having different band gap energies. In this case, the threshold of the LD device can be decreased by performing so-called modulated doping, i.e., doping either the first layer or the second layer with an impurity at a higher concentration. For example, this p-side cladding layer **218** can be formed by alternately stacking first thin layers made of AlGaN doped with a p-type impurity, e.g., Mg, and second thin layers made of undoped GaN. The p-side cladding layer **218** is preferably formed to have a thickness from 100 angstroms to 2 μm, and more preferably from 500 angstroms to 1 μm.

To decrease the forward voltage Vf of the LD device, making the p-side cladding layer **218** have a superlattice structure is preferable to make the n-side cladding layer **213** have a superlattice structure because the resistance of each p-side layer tends to decrease.

In a nitride semiconductor device having a double-hetero structure including the active layer **215** having a quantum structure, especially an LD device, it. is very preferable that the cap layer **216** having a band gap energy higher than that of the active layer **215** and a thickness of 0.1 μm or less and containing an aluminum-containing nitride semiconductor be formed in contact with the active layer **215**, the p-side light guide layer **217** having a band gap energy lower than that of the cap layer **216** and containing a nitride semiconductor be formed at a greater distance from the active layer **85** than the cap layer **86**, and the p-side cladding layer **218** having a band gap energy higher than that of the p-side light guide layer **217**, containing an aluminum-containing nitride semiconductor, and having a superlattice structure be formed at a greater distance from the active layer **215** than the p-side light guide layer **217**. In this case, since the p-side cap layer **216** has a larger band gap energy, the electrons injected from the n-side layer are blocked by the cap layer **216**. As a result, the electrons do not overflow the active layer **215**, and hence the leakage current of the LD device is reduced.

The LD device structure is basically made up of the n-side cladding layer **213**, the n-side light guide layer **214**, the active layer **215**, the p-side light guide layer **217**, and the p-side cladding layer **218**.

In addition, a p-side contact layer **219** made of a p-type nitride semiconductor is formed on the p-side cladding layer **218** to mount a p-electrode. This p-side contact layer **219** is preferably made of $In_aAl_bGa_{1-a-b}N$ ($0 \leqq x$, $0 \leqq y$, $x+y \leqq 1$) doped with a p-type impurity, especially GaN doped with a p-type impurity, especially Mg. The p-side contact layer **219** is preferably formed to have a thickness of 500 angstroms or less, more preferably from 20 angstroms and 400 angstroms.

As shown in FIG. **10**, the p-side contact layer **219** as the uppermost layer and part of the p-side cladding layer **218** are etched in the form of stripes to form a ridge. A p-side electrode **220** is formed on the entire surface of the top surface of this ridge. The p-side electrode **220** is preferably made of Ni, Pt, Pd, Co, Ni/Au (multilayer or alloy), Pt/Au (multilayer or alloy), or Pd/Au (multilayer or alloy) to achieve more desirable ohmic contact with the p-side contact layer **219**.

An insulating film **221** preferably made of SiO_2 or ZrO_2 is formed on the exposed surfaces of the p-side cladding layer **218** and the p-side contact layer **219** except for the top surface of the p-side electrode **220**. A p-side pad **222** electrically connected to the p-side electrode **220** through this insulating film **221** is formed.

Furthermore, as described above, the nitride semiconductor substrate **1000** has been doped with an n-type impurity to form an n-side electrode **223** on almost the entire lower surface of the substrate. If the n-side electrode **223** is made of a metal such as Al, Ti, W, Cu, Zn, Sn, or In, a multilayer made of these metals, or an alloy of the metals, more desirable ohmic contact with an n-type layer (the lower surface of the substrate **1000** in this case) can be achieved. As a metellization for mounting a heat sink (not shown) on the n-side electrode **223**, a thin metal film (not shown) having a two-layer structure preferably made of Au/Sn is formed.

FIG. **11** is a schematic perspective view showing an LD device having a structure similar to that shown in FIG. **10** except that a nitride semiconductor substrate **1000** supported on a support member **10** supports the LD device. In the LD device shown in FIG. **11**, except for a ridge, a p-side cladding layer **218**, a p-side light guide layer **217**, a cap layer **216**, an active layer **215**, an n-side light guide layer **214**, an n-side cladding layer **213**, and a crack prevention layer **212** are etched to expose their side surfaces, thereby providing a

rectangular parallelepiped structure. This etching reaches a portion in the surface of a buffer layer **211** to expose the surface portions of the buffer layer **211** on the two sides of the rectangular parallelepiped structure. N-side electrodes **223***a* and **223***b* are formed on the two exposed surface portions of the buffer layer **211** (in this case, the buffer layer **211** also serves as an n-side contact layer). Obviously, an insulating film **221** covers the exposed side surfaces of the p-side cladding layer **218**, the p-side light guide layer **217**, the cap layer **216**, the active layer **215**, the n-side light guide layer **214**, the n-side cladding layer **213**, and the crack prevention layer **212**. When the substrate **1000** is doped with an n-type impurity, the buffer layer **211** may be completely etched by the above etching to expose the surface of the substrate **1000**. In this case, the n-side electrodes **223***a* and **223***b* can be formed on the exposed surface of the substrate **1000**. In addition, an n-side electrode may be formed on only one side of the above rectangular parallelepiped structure.

FIG. **12** shows the structure of still another LD device according to the present invention. In the LD device shown in FIG. **12**, an insulating film **221** is formed thick on the exposed surface of a p-side cladding layer **218** such that the top surface of a p-side contact layer **219** is exposed. This LD device has a structure similar to that of the LD device in FIG. **11** except that the pad electrode **222** is not formed because a p-side electrode **220** is formed, in contact with the p-side contact layer **219**, on a wide region of the insulating film **221**. In addition, in the LD device in FIG. **12**, only one n-side electrode **223** is formed.

A nitride semiconductor as an element of the nitride semiconductor device structure of the present invention can be grown by using any of known methods suitable for the growth of a nitride semiconductor such as MOVPE, HVPE, and MBE. The MOVPE method is a preferable growth method. This method can grow an excellent crystal. However, since the MOCVD method takes a long period of time, a thicker nitride semiconductor layer is preferably formed by a method taking a relatively short period of time for crystal growth. In addition, nitride semiconductor portions are preferably grown by properly selecting various nitride semiconductor growth methods depending on the application purposes. In doping a nitride semiconductor with an n-type impurity or a p-type impurity, as is known well in this field, a Group IV element in the form of an organic compound or a hydride can be used as an n-type impurity, and a Group II element in the form of an organic compound can be used as a p-type impurity.

The present invention will be described below with reference to examples. In each of the following examples, MOVPE was performed under a reduced pressure of 50 to 400 Torr.

EXAMPLE 1

This example will be described with reference to FIGS. **1**A to **1**C.

First of all, a striped photomask was formed on a sapphire substrate **11**, 2 inches in diameter, having a C plane as a major surface and an ORF surface forming an A plane, and 0.1-μm thick selective growth masks **13** made of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval (width of each window) of 6 μm were formed by using a CVD apparatus. The respective stripe masks were formed to extend parallel in a direction perpendicular to the ORF surface.

The sapphire substrate **11**, on which the selective growth masks **13** were formed, was set in an MOVPE reaction vessel. A low-temperature buffer layer (not shown) made of GaN was then grown on the substrate **11**, on which the selective growth masks **11** were formed, to a thickness of about 200 angstroms at a temperature of 510° C. by using hydrogen as a carrier gas and ammonia and TMG as source gases. This low-temperature buffer layer was formed in only windows **14**.

After the buffer layer was grown, only the flow of TMG was stopped (i.e., hydrogen carrier gas and ammonia were kept fed), and the temperature was raised to 1105° C. At 1,050° C., a nitride semiconductor crystal substrate **16** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 100 μm by using TMG and ammonia as source gases and silane gas as a dopant gas.

Subsequently, the wafer, on which the GaN crystal substrate was grown, was removed from the reaction vessel, and the surface of the GaN crystal substrate **16** was formed into a mirror surface by lapping.

COMPARATIVE EXAMPLE 1

For comparison, a GaN buffer layer was directly grown on a sapphire substrate as in Example 1 to a thickness of 200 angstroms, in the same manner as described above, without forming the selective growth masks **13**. GaN doped with Si at $1\times10^{18}/cm^3$ was then grown on the buffer layer to a thickness of 100 μm in the same manner as described above.

When the number of lattice defects (crystal defects) per unit area in the GaN crystal obtained in Example 1 and that in the GaN crystal obtained in Comparative Example 1 were measured by two-dimensional TEM observation, the number of lattice defects in the GaN crystal in Example 1 was 1/10 or less that in Comparative Example 1.

EXAMPLE 2

This example will be described with reference to FIGS. **6**A to **6**C.

Second selective growth masks **113** having a stripe width of 10 μm and a stripe interval of 6 μm were grown on the surface of a GaN crystal **16** obtained as in Example 1 to a thickness of 0.1 μm in the same manner as in Example 1. The positions of the second selective growth masks **113** were shifted from those of first selective growth masks **13**. More specifically, mask alignment was performed such that the respective stripes of the second selective growth masks **113** were located at positions corresponding to windows **14** of the first selective growth masks and extend parallel to the first selective growth masks **13**.

The wafer, on which the second selective growth masks **113** were formed, was placed back into the MOVPE reaction vessel, and a GaN crystal **116** doped with Si at: $1\times10^{18}/cm^3$ was grown to a thickness of 150 μm by using TMG and ammonia as source gases and silane gas as a dopant gas.

The wafer, on which the GaN crystal **116** was grown, was removed from the reaction vessel. The surface of the crystal was then mirror-polished, and the number of lattice defects (crystal defects) per unit area was measured by two-dimensional TEM observation in the same manner as in Example 1. The number of defects in the GaN crystal **116** in this example was 1/100 or less that in the GaN crystal in Comparative Example 1.

EXAMPLE 3

This example will be described with reference to FIGS. **1**A to **1**C and **6**A to **6**C.

A low-temperature buffer layer made of GaN was grown on a sapphire substrate **11** as in Example 1 to a thickness of

200 angstroms, and an undoped GaN layer was grown on the buffer layer to a thickness of 5 μm, thereby forming an underlayer **12** having a two-layer structure. First selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval of 8 μm were grown on the flat surface of the underlayer **12** of a support member **10**, obtained in this manner, to a thickness of 0.1 μm by the same method as in Example 1. The first selective growth masks **13** extended parallel in a direction perpendicular to the sapphire A plane.

The wafer, on which the first selective growth masks **13** were formed, was moved into the MOVPE reaction vessel. An undoped GaN crystal **16** was then grown on the wafer to a thickness of 10 μm at 1,050° C. by using TMG and ammonia as source gases.

The wafer, on which the GaN crystal **16** was grown, was removed from the reaction vessel, and the surface of the GaN crystal **16** was formed into a mirror surface by lapping. Second selective growth masks **113** made up of many Si_3N_4 stripes having a stripe width of 12 μm and a stripe interval of 6 μm were grown on the surface of this GaN crystal **16** to a thickness of 0.1 μm by the same method as in Example 1. The respective second strip masks were formed at positions corresponding to windows **14** of the first selective growth masks.

The wafer, on which the second selective growth masks **113** were formed, was placed back into the MOVPE reaction vessel, and an undoped GaN crystal **116** was grown to a thickness of 150 μm. The number of crystal defects in the obtained undoped GaN crystal **116** was almost equal to that in the GaN crystal in Example 2.

EXAMPLE 4

An Si-doped GaN crystal **16** was grown to a thickness of 100 μm by the same method as in Example 1 except that a sapphire substrate having an A plane as a major surface and an ORF surface forming an R plane was used, and silicon dioxide stripe masks were formed to extend in a direction perpendicular to the R plane. The number of crystal defects in this GaN crystal **16** was almost equal to that in the GaN crystal in Example 1.

EXAMPLE 5

This example will be described with reference to FIGS. **1**A to **1**C.

A spinnel substrate **11**, 1 inch in diameter, having a (211) plane as a major surface and an ORF surface forming a (110) plane was prepared. First selective growth masks **13** made up of many SiO_2 stripes were formed on the surface of this spinnel substrate **11** to extend in a direction perpendicular to the ORF surface. The stripe width was 12 μm, and the stripe interval was 6 μm.

A quartz boat having Ga metal accommodated in a quartz reaction vessel was placed in the HVPE apparatus. The spinnel substrate **11**, on which the first selective growth masks **13** were formed, was tilted at a position apart from the quartz boat. A halogen gas feed pipe was placed near the Ga metal in the reaction vessel, and a nitrogen source feed pipe was placed near the substrate **11**.

HCl gas was fed into the reaction vessel, together with a nitrogen carrier gas, through the halogen gas feed pipe. In this case, the boat accommodating the Ga metal was heated to 900° C., and the spinnel substrate was heated to 1,050° C. The HCl gas was then caused to react with the Ga metal to produce $GaCl_3$. Ammonia gas was fed into the reaction vessel, together with a nitrogen carrier gas, through the nitrogen source feed pipe near the spinnel substrate **11**, and silane gas was fed, together with hydrogen chloride gas, through the halogen gas feed pipe. Crystal growth was then performed for 3 hours at a growth rate of 50 μm/h. As a result, a GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 150 μm.

The wafer, on which the HVPE gallium nitride crystal **16** was grown, was removed from the reaction vessel. The uneven portions on the surface of the GaN crystal **16** were removed by lapping, and the number of lattice defects was measured. The number of defects in the GaN crystal **16** obtained in this example was equal to that in the GaN crystal in Example 1.

EXAMPLE 6

This example will be described with reference to FIGS. **8**A and **8**B.

A wafer having the Si-doped GaN crystal obtained in Example 1 was set in the reaction vessel of the MOVPE apparatus, and a high-temperature buffer layer **81** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on the Si-doped GaN crystal to a thickness of 1 μm at 1,050° C.

Subsequently, a 20-angstroms thick active layer **82** made of $In_{0.4}Ga_{0.6}N$ and having a single quantum well structure, a 0.3-μm thick p-side cladding layer **83** made of Mg-doped $Al_{0.2}Ga_{0.8}N$, and a 0.5-μm thick p-side contact layer **84** made of Mg-doped GaN were sequentially grown on the high-temperature buffer **81** by MOVPE.

After this step, the wafer was removed from the reaction vessel and annealed in a nitrogen atmosphere at 600° C. to reduce the resistances of the p-side cladding layer **83** and the p-side contact layer **84**.

Etching was sequentially performed from the p-side contact layer **84** to partly expose the Si-doped GaN crystal. This etching provides a "cutting margin" in a, subsequent scribing process.

After etching, a 200-angstroms thick light-transmitting p-side electrode **85** having a two-layer structure made of Ni/Au was formed on almost the entire surface of the p-side contact layer **84**. A 0.5-μm thick pad electrode **86** for bonding was formed on the p-side electrode **85**.

After the pad electrode **86** was formed, a sapphire substrate **11** of the wafer, a low-temperature buffer layer **12**, and first selective growth masks **13** (see FIG. 1C) were removed by polishing to expose the lower surface of an Si-doped GaN crystal **16**. A 0.5-μm thick n-side electrode **87** was formed on almost the entire lower surface.

Subsequently, scribing was performed from the n-electrode side along the above cutting margin to cleave the M plane ($(1\bar{1}00)$ plane) of the Si-doped GaN crystal **16** from a plane perpendicular to the M plane, thereby obtaining a 300-μm square LED chip. This LED emitted 520-nm green light with 20 mA. The output level and electrostatic breakdown voltage of the LED were twice or more those of the LED device grown on a conventional sapphire substrate. That is, this device exhibited excellent characteristics.

EXAMPLE 7

This example will be described with reference to FIG. **10**.

A wafer, on which an Si-doped GaN crystal **116** obtained in as Example 2 was grown, was set in the MOVPE reaction vessel of the MOVPE apparatus, and a high-temperature buffer layer **211** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on the Si-doped GaN crystal **116** to a thickness of 1 μm at 1,050° C.

A crack prevention layer **212** made of $In_{0.1}Ga_{0.9}N$ doped with Si at $5\times10^{18}/cm^3$ was grown on the high-temperature buffer layer **211** to a thickness of 500 angstroms.

An n-side cladding layer **213** having a total thickness of 0.4 μm and a superlattice structure was formed on the crack prevention layer **212** by alternately stacking a total of 100 20-angstroms thick first layers, each made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $5\times10^{18}/cm^3$, and 20-angstroms thick second layers, each made of undoped GaN.

An n-side light guide layer **214** made of n-type GaN doped with Si at $5\times10^{18}/cm^3$ was grown on the n-side cladding layer **213** to a thickness of 0.1 μm.

Subsequently, 25-angstroms thick well layers made of undoped $In_{0.2}Ga_{0.8}N$ and 50-angstroms thick barrier layers made of undoped $In_{0.0}Ga_{0.95}N$ were alternately stacked to form an active layer **215** having a total thickness of 175 angstroms and a multi quantum well (MQW) structure.

A p-side cap layer **216** made of p-type $Al_{0.3}Ga_{0.9}N$ doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of a p-side light guide layer **217** and that of the active layer **215** was grown to a thickness of 300 angstroms.

The p-side light guide layer **217** made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of the p-side cap layer **216** was grown on the p-side cap layer **216** to a thickness of 0.1 μm.

Subsequently, 20-angstroms thick first layers made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$ and 20-angstroms thick second layers made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ were alternately stacked on the p-side light guide layer **217** to form a p-side cladding layer **218** having a total thickness of 0.4 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $2\times10^{20}/cm^3$ was grown to a thickness of 150 angstroms.

After all the nitride semiconductor layers were grown, the wafer was annealed in a nitrogen atmosphere at 700° C. in the reaction vessel, thereby further decreasing the resistance of each p-type layer. After annealing, the wafer was removed from the reaction vessel, and the p-side contact layer **219** as the uppermost layer and the p-side cladding layer **218** were etched by using an RIE apparatus, so that a 4-μm wide striped ridge was formed. A p-side electrode **220** having a two-layer structure made of Ni/Au was formed on the entire top surface of the ridge. An insulating film **221** made of SiO_2 was formed on the exposed side surfaces of the p-side cladding layer **218** and the contact layer **219** except for the p-side electrode **220**. A p-side pad electrode **222** electrically connected to the p-side electrode **220** was formed through this insulating film **221**.

After the p-side pad electrode **222** was formed, a sapphire substrate **11** of the wafer, a buffer layer **12**, first selective growth masks **13**, a first GaN crystal **16**, second selective growth masks **113**, and part of the second GaN crystal **116** were removed by polishing to expose the lower surface of the second GaN crystal. A 0.5-μm thick n-side electrode **223** having a two-layer structure made of Ti/Al was formed on the entire lower surface of the second GaN crystal. A thin Au/Sn film for metallization for a heat sink was formed on the n-side electrode **223**.

Subsequently, the wafer was scribed from the n-side electrode **223** to cleave the second GaN crystal **116** in the form of a bar from the M plane ($(1\bar{1}00)$ plane) of the second GaN crystal **116** corresponding to a side surface of a hexagonal prism in FIG. **3**, thereby manufacturing a resonance surface. A dielectric multilayer film made of SiO_2 and TiO_2 was formed on this resonance surface. Finally, the bar was cut in a direction parallel to the extending direction of the p-side electrode **220** to obtain laser chips. When the LD device product obtained by placing the respective chips on the heat sink with the chips facing up (in a state wherein the substrate faces the heat sink), and performing wire bonding for the p-side pad **222** was laser-oscillated at room temperature, continuous oscillation of an oscillation wavelength of 405 nm was observed at room temperature, a threshold current density of 2.0 k/cm^2, and a threshold voltage of 4.0V. This product exhibited an oscillation life of 1,000 hrs or more.

EXAMPLE 8

This example will be described with reference to FIG. **9**.

On an undoped GaN crystal **116** obtained as in Example 2, a high-temperature buffer layer **81** made of GaN doped with Si at $1\times10^{18}/cm^3$, a 20-angstroms thick active layer **82** made of $In_{0.4}Ga_{0.6}N$ and having a single quantum well structure, a 0.3-μm thick p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg, and a 0.5-μm thick p-side contact layer **84** made of Mg-doped GaN were sequentially grown by the same method as in Example 6. A light-transmitting p-side electrode **85** was formed on almost the entire surface of the p-side contact layer **84** in the same manner as in Example 6. A pad electrode **86** was formed on the p-electrode **85**. After a predetermine etching step, an n-side electrode **87** was formed on the high-temperature buffer layer **81**.

The LED device of this example differs from the LED device of Example 6 in that the LED device structure of this example is formed on the second GaN crystal **116** having better crystallinity than the GaN crystal **116** of Example 1, and the p-side electrode **85** and the n-side electrode **87** are formed on the same surface side of the substrate. In a nitride semiconductor device having a structure in which a nitride semiconductor doped with an n-type impurity (high-temperature buffer layer **81**) is stacked on an undoped GaN crystal substrate in this manner, when an n-electrode is formed on the n-type layer side, an LED device with low Vf and high emission efficiency tends to be easily obtained by forming the n-electrode on the nitride semiconductor layer doped with an n-type impurity. In fact, both the output level and electrostatic breakdown voltage of the LED device of Example 8 increased about 1.5 times those of the LED device of Example 6.

EXAMPLE 9

This example will be described with reference to FIGS. **1A** to **1C** and **9**.

Similar to Example 3, a 200-angstroms thick low-temperature buffer layer made of GaN and a 4-μm thick undoped GaN layer were grown on a sapphire substrate **11** having a C plane as a major surface and an ORF surface forming an A plane so as to form an underlayer **12** having a tow-layer structure. First selective growth masks made up of many SiO_2 stripes having a stripe width of 20 μm and a stripe interval of 5 μm were grown on the undoped GaN layer to a thickness of 0.1 μm by using a CVD apparatus. The first selective growth masks extended parallel in a direction perpendicular to the ORF surface.

This wafer was transferred to the MOVPE apparatus, and a GaN crystal doped with Si at $1\times10^{19}/cm^3$ was grown to a thickness of 15 μm.

Subsequently, in the same manner as in Example 8, a high-temperature buffer layer made of GaN doped with Si at

$1\times10^{18}/cm^3$, a 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer having a single quantum well structure, a 0.3-μm thick p-side cladding layer made of Mg-doped $Al_{0.2}Ga_{0.8}N$, and a 0.5-μm thick p-side contact layer made of Mg-doped GaN were sequentially grown on the Si-doped GaN crystal. Thereafter, etching was performed from the p-side cladding layer to expose the surface of the Si-doped GaN crystal having a high impurity concentration, and an n-side electrode was formed on the exposed surface. A light-transmitting p-side electrode was formed on almost the entire surface of the p-side contact layer. A pad electrode for bonding was formed on the p-side electrode. As described above, in this LED device, the n- and p-side electrodes were formed on the same surface of the substrate. Finally, the sapphire substrate was thinned to a thickness of about 50 μm by polishing, and scribing was performed on the polished surface side to obtain a 350-μm square LED device. This LED device exhibited characteristics almost equivalent to those of the LED device of Example 6, but the yield of device itself was 100 times or more that in Example 6.

EXAMPLE 10

This example will be described with reference to FIGS. **1**A to **1**C, **2**, and **9**.

A sapphire substrate **11**, 2 inches diameter, having an off angle θ=0.13° from the C plane, a step difference of about 15 angstroms, steps each having a terrace width W of about 56 angstroms, and an ORF surface forming an A plane was prepared.

Similar to Example 9, a low-temperature buffer layer made of GaN was grown on the off-angled surface of this sapphire substrate to a thickness of 200 angstroms, and an undoped GaN layer was grown on the buffer layer to a thickness of 4 μm to form an underlayer **12** having a two-layer structure. Thereafter, first selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 25 μm and a stripe interval of 5 μm were grown on this undoped GaN layer to a thickness of 0.1 μm. The first selective growth masks extended parallel in a direction perpendicular to the A plane.

This wafer was transferred to the MOVPE apparatus, and a GaN crystal doped with Si at $1\times10^{19}/cm^3$ was grown on the wafer to a thickness of 10 μm.

A high-temperature buffer layer made of GaN doped with Si at $1\times10^{18}/cm^3$, a 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer having a single quantum well structure, a 0.3-μm thick p-side cladding layer made of Mg-doped $Al_{0.2}Ga_{0.8}N$, and 0.5-μm thick a p-side contact layer made of Mg-doped GaN were sequentially grown on the Si-doped GaN crystal.

Subsequently, a 350-μm square LED device was obtained by performing the same processing as that in Example 9. The output level of this LED device improved 5% as compared with the LED device of Example 9, and the yield of the device itself was high as in Example 9.

EXAMPLE 11

After a GaN crystal doped with Si at $1\times10^{19}/cm^3$ was grown to a thickness of 10 μm following the same procedure as in Example 9, the wafer was removed from the reaction vessel of the MOVPE apparatus, and 0.1-μm thick second selective growth masks made up of silicon dioxide stripes, each having a stripe width of 15 μm, were formed at positions corresponding to the window portions of the first selective growth masks. The wafer, on which the second selective growth masks were formed, was transferred to the MOVPE apparatus, and a second GaN crystal **116** doped with Si at $1\times10^{19}/cm^3$ was grown to a thickness of 15 μm.

Subsequently, in the same manner as in Example 9, a high-temperature buffer layer made of GaN doped with Si at $1\times10^{18}/cm^3$, a 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer having a single quantum well structure, a 0.3-μm thick p-side cladding layer made of Mg-doped $Al_{0.2}Ga_{0.8}N$, and a 0.5-μm thick p-side contact layer made of Mg-doped GaN were sequentially grown on the second Si-doped GaN crystal **116**. Thereafter, a 350-μm square LED device was obtained by following the same procedure as in Example 9. This LED device exhibited almost the same characteristics as those of the LED device of Example 8. The yield of the device itself was 100 times or more that in Example 8.

EXAMPLE 12

This example will be described with reference to FIGS. **8**A and **8**B, in particular.

A sapphire substrate **11** having a C plane as a major surface and an ORF surface forming an A plane was set in the reaction vessel of the MOVPE apparatus, and a low-temperature buffer layer made of GaN was grown on the sapphire substrate **11** to a thickness of 200 angstroms at 500° C. Thereafter, the temperature in the reaction vessel was set to 1,050° C. to grow a GaN layer to a thickness of 5 μm, thereby forming an underlayer **12** having a two-layer structure.

This wafer was removed from the reaction vessel. Stripe photomasks were then formed on the top surface of the underlayer **12**. Selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 20 μm and a stripe interval (width of each window) of 5 μm were formed to have a thickness of 0.1 μm by using a CVD apparatus. The respective stripe masks extended parallel in a direction perpendicular to the ORF surface.

The wafer, on which the first selective growth masks **13** were formed, was set in the MOVPE reaction vessel again, and a GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 100 μm at 1,050° C.

The wafer, on which the Si-doped GaN crystal **16** was grown, was removed from the MOVPE reaction vessel, and the surface of the Si-doped GaN crystal **16** was formed into a mirror surface by lapping. The number of crystal defects in the surface region, of this Si-doped GaN crystal **16**, which corresponds to each first selective growth mask **13** was $10^6/cm^2$ or less.

The wafer, on which the Si-doped GaN crystal **16** was grown, was transferred to the MOVPE reaction vessel again, and a buffer layer (n-side cladding layer) **81** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on the Si-doped GaN crystal **16** to a thickness of 1 μm.

Subsequently, a 20-angstroms thick undoped $In_{0.4}Ga_{0.6}N$ active layer **82** having a single quantum well structure, a 0.3-μm thick p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$, and a 0.5-μm thick p-side contact layer **84** made of GaN doped with Mg at $1\times10^{20}/cm^3$ were sequentially grown on the n-side cladding layer **81**.

After this step, the wafer was removed from the MOVPE reaction vessel and annealed in a nitrogen atmosphere at 600° C. to reduce the resistances of the p-side cladding layer **83** and the p-side contact layer **84**. Etching was then performed from the p-side contact layer **84** to expose the surface of the n-side cladding layer **81** or the GaN crystal **16**, and a cutting margin was formed.

After the etching step, a 200-angstroms thick light-transmitting p-side electrode **85** having a two-layer structure

made of Ni/Au was formed on almost the entire surface of the p-side contact layer **84**, and a 0.5-μm thick p-side pad electrode **86** for bonding was formed on the p-electrode **85**.

After the p-side pad electrode **86** was formed, the sapphire substrate **11** of the wafer, the underlayer **12**, and the first selective growth masks **13** were removed by polishing to expose the lower surface of the GaN crystal **16**, and a 0.5-μm thick n-side electrode **87** having a two-layer structure made of W/Al was formed on almost the entire lower surface.

Subsequently, the wafer was cut along the cutting margin into a bar, and the bar was cut in a direction perpendicular to a short side of the bar to obtain an LED chip. The crystal defects in the nitride semiconductor layer under the active layer of this LED chip were few in a portion on each first selective growth mask, and were many in a portion on each window portion. A highly reliable device can therefore be obtained by setting a large area of the active layer in the regions having few crystal defects. The LED obtained in this example emitted 520-nm green light with 20 mA. The output level and electrostatic breakdown voltage of the LED were twice or more those of a nitride semiconductor device structure grown on a conventional sapphire substrate. That is, this device exhibited excellent characteristics.

In this example, each first selective growth mask was in the form of a stripe. However, selective growth masks may be formed in advance to have a regular dot pattern in accordance with the shape of each chip to be cut (e.g., a rectangular shape), and chips may be cut at positions corresponding to the window portions of the selective growth masks.

EXAMPLE 13

This example will be described with reference to FIG. **11**, in particular.

A GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 6 μm by the same method as in Example 12.

The wafer, on which this GaN crystal **16** was grown, was set in the MOVPE reaction vessel, and a high-temperature buffer layer **211** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on this Si-doped GaN crystal **15** at 1,050° C.

A crack prevention layer **212** made of $In_{0.1}Ga_{0.8}N$ doped with Si at $5\times10^{18}/cm^3$ was grown on the high-temperature buffer layer **211** to a thickness of 500 angstroms.

Subsequently, a total of 10 20-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $5\times10^{18}/cm^3$ and 20-angstroms thick second layers made of undoped GaN were alternately stacked on the crack prevention layer **212** to form an n-side cladding layer **213** having a total thickness of 0.4 μm and a superlattice structure.

An n-side light guide layer **214** made of n-type GaIl doped with Si at $5\times10^{18}/cm^3$ was grown to a thickness of 0.1 μm.

Twenty-five-angstroms thick well layers made of undoped $In_{0.2}Ga_{0.8}N$ and 50-angstroms thick barrier layers made of undoped $In_{0.01}Ga_{0.99}N$ were alternately stacked on the n-side light guide layer **214** to form an active layer **215** having a total thickness of 175 angstroms and a multi quantum well (MQW) structure.

A p-side cap layer **216** made of p-type $Al_{0.3}Ga_{0.7}N$ doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of a p-side light guide layer **217** and that of the active layer **215** was grown on the active layer **215** to a thickness of 300 angstroms.

The p-side light guide layer **217** made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy lower than that of the p-side cap layer **216** was grown on the p-side cap layer **216** to a thickness of 0.1 μm.

Twenty-angstroms thick first layers made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$ and 20-angstroms thick second layers made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ were alternately stacked on the p-side light guide layer **217** to grow a p-side cladding layer **218** having a total thickness of 0.4 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $2\times10^{20}/cm^3$ was grown to a thickness of 150 angstroms.

After all the nitride semiconductor layers were grown, the wafer was annealed in a nitrogen atmosphere at 700° C. in the reaction vessel to further decrease the resistance of each p-type layer. After the annealing step, the wafer was removed from the reaction vessel, and the p-side contact layer **219** as the uppermost layer and the p-side cladding layer **218** were etched by using an RIE apparatus to form a ridge having a stripe with of 4 μm. The ridge was formed above the first selective growth masks in a direction parallel to the stripes of the first selective growth masks.

After the ridge was formed, the portions, of the p-side light guide layer **217**, which were exposed on the two sides of the ridge stripe were etched to expose the surface portions, of the n-side cladding layer **211**, on which n-side electrodes **223***a* and **223***b* were to be formed.

After this step, a p-side electrode **220** having a two-layer structure made of Ni/Au was formed on the entire top surface of the ridge. An insulating film **221** made of SiO_2 was formed on the surfaces of the p-side cladding layer **218** and the p-side contact layer **219** except for the p-side electrode **220**. A p-side pad electrode **222** electrically connected to the p-side electrode **220** through the insulating film **221** was formed. The n-side electrodes **223***a* and **223***b* having a two-layer structure made of W/Al were formed on the exposed surfaces of the n-side cladding layer **211**.

After the n-side electrode was formed, the sapphire substrate of the wafer was polished to a thickness of 50 μm in the same manner as in Example 1. Thereafter, the active layer **215** was cleaved from the sapphire substrate **11** in a direction perpendicular to the p-side electrode **220** and the n-side electrodes **223***a* and **223***b* in the form of stripes, thereby making the cleavage surface of the active layer **215** serve as a resonance surface. The GaN crystal **16** includes regions having many crystal defects and regions having few crystal defects. In an LD device, the n-side electrodes **223***a* and **223***b* were formed on the regions having many crystal defects to omit the active layer **215**. Since this eliminates the possibility that the active layer **215** on which heat concentrates is destroyed by crystal defects, a highly reliable LD device having a long service life can be realized.

When the LD device obtained in this example was laser-oscillated at room temperature, continuous oscillation of an oscillation wavelength of 405 nm was observed at a threshold current density of 2.0 kA/cm^2 and a threshold voltage of 4.0V. This product exhibited an oscillation life of 1,000 hrs or more.

EXAMPLE 14

This example will be described with reference to FIGS. **1**A to 1C, in particular.

First of all, a striped photomask was formed on a sapphire substrate **11**, 2 inches in diameters, having a C plane as a major surface and an ORF surface forming an A plane by the same method as in Example 1, and first selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval (window **14**) of 5 μm

were grown to a thickness of 1 μm. The respective stripes **13** extended in a direction perpendicular to the ORF surface of the sapphire substrate **11**.

The sapphire substrate **11**, on which the first selective growth masks **13** were formed, was set in the MOVPE reaction vessel, and a low-temperature buffer layer (not shown) made of GaN was grown on the substrate **1**, on which the selective growth masks **13** were formed, to a thickness of about 20 angstroms by setting a temperature of 510° and using hydrogen as a carrier gas and ammonia and TMG as source gases.

After the buffer layer was grown, only the flow of TMG was stopped, and the temperature was raised to 1,050° C. A GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 100 μm at 1,050° C. by using TMG and ammonia as source gases and silane gas as a dopant gas.

After this step, the wafer on which the GaN crystal **16** was grown was removed from the reaction vessel, and the surface of the GaN crystal (substrate) **16** was formed into a mirror surface by lapping.

The number of crystal defects in the GaN crystal obtained in Example 14 and that in the GaN crystal obtained in Comparative Example 1 were measured by two-dimensional TEM observation. As a result, the average number of crystal defects in the GaN crystal obtained in Example 14 was $1.3\times10^6/cm^2$, and that in the GaN crystal in Comparative Example 1 was $2.4\times10^7/cm^2$. The number of crystal defects in the GaN crystal of Example 14 was 1/10 or less that in the GaN crystal in Comparative Example 1.

EXAMPLE 15

This example will be described with reference to FIGS. **1A** to **1C**.

A low-temperature buffer layer made of GaN was grown on the sapphire substrate **11** used in Example 14 to a thickness of 200 angstroms, and an undoped GaN layer was grown on the buffer layer to a thickness of 5 μm, thereby forming an underlayer **12** having a two-layer structure. One-μm thick first selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval of 3 μm were formed on the top surface of the underlayer **12** of this wafer by the same method as in Example 14. The respective stripes **13** extended in a direction perpendicular to the ORF surface of the sapphire substrate **11**.

The wafer, on which the selective growth masks **13** were formed, was transferred to the HVPE reaction vessel, and an Si-doped GaN crystal **16** was grown on the wafer to a thickness of 300 μm at 1,050° C. by using $GaCl_3$ and ammonia as source gases and silane gas as a dopant gas.

The wafer, on which the GaN crystal **16** was grown, was removed from the reaction vessel. The sapphire substrate **11**, the underlayer **12**, and the sapphire substrate **11** were removed by polishing, and the lower surface of the GaN crystal **16** was mirror-finished, thereby obtaining an Si-doped GaN crystal substrate.

As in Example 14, when the number of crystal defects in the surface of the substrate on the opposite side to the polished surface was measured, the number was $1\times10^3/cm^2$, which was smaller than that in the GaN crystal of Example 14. That is, a device manufacturing substrate having very good crystallinity was obtained.

EXAMPLE 16

An Si-doped GaN crystal **16** was grown to a thickness of 100 μm by the same method as in Example 14 except that the sapphire substrate **11** having an A plane as a major surface and an ORF surface forming an R plane was used as the dissimilar substrate **11**. Note that stripes **13** extended in a direction perpendicular to the R plane. As a result, the GaN crystal **16** having very few etching pits, which were almost equal in number to those in Example 1, was obtained.

EXAMPLE 17

A spinnel substrate **11**, 1 inch in diameter, having a (111) plane as a major surface and a (110) plane forming an ORF surface was prepared. One-μm thick first selective growth masks **13** made up of many SiO_2 stripes were formed on the surface of this spinnel substrate **1** to extend in a direction perpendicular to the ORF surface by the same method as in Example 1. The strip width was 10 μm, and the stripe interval was 3 μm.

A GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown on the spinnel substrate **11**, on which the selective growth masks **13** were formed, to a thickness of 150 μm by the same HVPE method as that in Example 5.

The wafer, on which the Si-doped GaN crystal was grown, was removed from the reaction vessel, and the spinnel substrate **11** and the selective growth masks **13** were removed by lapping. When the number of crystal defects in the resultant structure was measured in the same manner as in Example 14, the GaN crystal obtained in this example was a crystal having very few etching pits almost equal in number to those in Example 14.

EXAMPLE 18

This example will be described with reference to FIGS. **8A** and **8B**, in particular.

A sapphire substrate **11**, a low-temperature buffer layer, and selective growth masks **13** were removed from a wafer obtained as in Example 14 by polishing so as to expose the lower surface of the Si-doped GaN crystal, thereby obtaining an Si-doped GaN crystal substrate **1000** in a free state.

This Si-doped GaN crystal substrate **1000** was set in the reaction vessel of the MOVPE apparatus, and a high-temperature buffer layer **81** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on the surface of the substrate at 1,050° C.

A 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer **82** having a single quantum well structure, a 0.3-μm p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$, and a 0.5-μm thick p-side contact layer **84** made of GaN doped with Mg at $1\times10^{20}/cm^3$ were sequentially grown on the high-temperature buffer layer **81**.

The wafer, on which the respective nitride semiconductor layers were grown, was removed from the reaction vessel and was annealed in a nitrogen atmosphere at 600° C. to decrease the resistances of the p-side cladding layer **83** and the p-side contact layer **84**. Thereafter, etching was performed from the p-side contact layer **34** side to expose the upper surface of the Si-doped GaN crystal substrate **1000**. With this etching step, a "cutting margin" for chip cutting was formed.

After the above etching step, a 200-angstroms thick light-transmitting p-side electrode **85** having a two-layer structure made of Ni/Au was formed on almost the entire upper surface of the p-side contact layer **84**. A 0.5-μm thick pad electrode **86** for bonding was formed on the p-side electrode **85**.

After the pad electrode was formed, a 0.5-μm thick n-side electrode **87** was formed on the entire lower surface of the GaN crystal substrate **1000**.

After this step, scribing was performed from the n-electrode side along the above cutting margin to cleave the M plane ((1$\bar{1}$00) plane) of the GaN crystal substrate **1000** from a surface perpendicular to the M plane, thereby obtaining a 300-μm square LED chip. This LED emitted 520-nm green light with 20 mA. The output level and electrostatic breakdown voltage of the LED were twice or more those of a device obtained by growing a nitride semiconductor device structure on a conventional sapphire substrate. That is, this device exhibited excellent characteristics.

EXAMPLE 19

This example will be described with reference to FIG. **10**.

An Si-doped GaN crystal substrate **1000** in a free state, obtained as in Example 18, was set in the reaction vessel of the MOVPE apparatus, and an n-side cladding layer **213** was directly formed on the upper surface of this substrate **1000** without forming a buffer layer **211** and a crack prevention layer **212**. More specifically, a total of 100 20-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{19}/cm^3$ and 20-angstroms thick second layers made of undoped GaN were alternately grown to form an n-side cladding layer **213** having a total thickness of 0.4 μm and a superlattice structure.

An n-side light guide layer **214** made of n-type GaN doped with Si at $1\times10^{17}/cm^3$ was grown on the n-side cladding layer **213** to a thickness of 0.1 μm.

Subsequently, 25-angstroms thick well layers made of $In_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{17}/cm^3$ and 50-angstroms thick barrier layers made of $In_{0.01}Ga_{0.95}N$ doped with Si at $1\times10^{17}/cm^3$ were alternately stacked on the n-side light guide layer **214** to form an active layer **215** having a total thickness of 175 angstroms and a multi quantum well (MQW) structure.

A p-side cap layer **216** made of $Al_{0.3}Ga_{0.9}N$ doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of the p-side light guide layer **217** and that of the active layer **215** was grown on the active layer **215** to a thickness of 300 angstroms.

Subsequently, a p-side light guide layer **217** made of p-type GaN doped with Mg at $1\times10^{18}/cm^3$ and having a band gap energy lower than that of the p-side cap layer **216** was grown on the p-side cap layer **216** to a thickness of 0.1 μm.

Twenty-angstroms thick first layers made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$ and 20-angstroms thick second layers made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ were alternately stacked on the p-side light guide layer **217** to form a p-side cladding layer **218** having a total thickness of 0.4 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $2\times10^{20}/cm^3$ was grown on the p-side cladding layer **218** to a thickness of 150 angstroms.

The wafer, on which the respective nitride semiconductor layers were formed in this manner, was annealed in a nitrogen atmosphere at 700° C. to further decrease the resistance of each p-type layer. After the annealing step, the wafer was removed from the reaction vessel, and the p-side contact layer **219** as the uppermost layer and the p-side cladding layer **218** were etched by using the RIE apparatus to provide a ridge having a stripe width of 4 μm. A p-side electrode **220** having a two-layer structure made of Ni/Au was formed on the entire top surface of the ridge.

Thereafter, an insulating film **221** made of SiO_2 was formed on the exposed side surface of the p-side electrode **220** and the exposed surfaces of the p-side cladding layer **218** and the contact layer **219** except for the top surface of the p-side electrode **220**. A p-side pad electrode **222** electrically connected to the p-side electrode **220** through the insulating film **221** was formed.

After the p-side pad electrode **222** was formed, a 0.5-μm thick n-side electrode **223** having a two-layer structure made of Ti/Al was formed on the entire lower surface of the Si-doped GaN crystal substrate **1000**. A thin film made of Au/Sn was formed for metallization for a heat sink on the n-side electrode **223**.

Subsequently, the wafer was scribed from the n-side electrode **223** to cleave the GaN crystal substrate **1000** along the M plane ((1$\bar{1}$00) plane); corresponding to a side surface of the hexagonal prism in FIG. **3**) of the GaN crystal substrate **1000** to provide a resonance surface and obtain a bar. A dielectric multilayer film made of SiO_2 and TiO_2 was formed on both or one of the resonance surfaces of this bar. Finally, the bar was cut in a direction parallel to the extending direction of the p-side electrode **220** to obtain an LD device chip. This chip was placed on the heat sink with the chip facing up, and the p-side pad electrode **222** was bonded thereto by wire bonding. When this LD device was laser-oscillated at room temperature, continuous oscillation of an oscillation wavelength of 405 nm was observed at a threshold current density of 2.0 kA/cm^2 and a threshold voltage of 4.0V. The device exhibited a life of 1,000 hrs or more.

EXAMPLE 20

This example will be described with reference to FIG. **9**, in particular.

A total of 100 20-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{19}/cm^3$ and 20-angstroms second layers made of undoped GaN were alternately grown on an undoped GaN crystal **16** (supported on sapphire substrate **11**) obtained as in Example 15 to form an n-side cladding layer **81** having a total thickness of 0.4 μm and a superlattice structure.

A 20-angstroms thick $In_{0.4}Ga_{0.6}N$ having a single quantum well structure, a 0.3-μm thick p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$, and a 0.5-μm thick p-side contact layer **84** made of GaN doped with Mg at $1\times10^{20}/cm^3$ were sequentially grown on the n-side buffer layer **81**. Etching was performed from the p-side contact layer **84** to expose the upper surface of the Si-doped GaN crystal **1000** having a high impurity concentration. An n-side electrode **87** was formed on the exposed upper surface. A light-transmitting p-side electrode **85** was formed on almost the entire surface of the p-side contact layer **84**. A pad electrode **86** for bonding was formed on the p-side electrode **85**. Finally, the sapphire substrate was polished to a thickness of about 50 μm, and the polished surface was scribed to obtain a 350-μm square LED device.

The output level and electrostatic breakdown voltage of the obtained LED device increased about 1.5 times those of the LED device of Example 18.

EXAMPLE 21

A low-temperature buffer layer made of GaN was grown on a sapphire substrate **11** as in Example 15 to a thickness of 200 angstroms following the same procedure as in Example 15. An undoped GaN layer was grown on the buffer layer to a thickness of 4 μm. Thereafter, first selective growth masks **13** identical to those in Example 15 were formed.

This wafer was transferred to the MOVPE apparatus, and a GaN crystal **16** doped with Si at $1\times10^{18}/cm^3$ was grown to a thickness of 15 μm.

After an n-side cladding layer **81**, an active layer **82**, a p-side cladding layer **83**, and a p-side contact layer **84** were sequentially grown on this GaN crystal **16** as in Example 20, the resultant structure was subjected to the same processing as that in Example 20, thereby obtaining a 350-μm square LED device. This LED device exhibited good characteristics like the LED device of Example 20. In addition, the service life of this LED device became longer than that of the LED device of Example 20.

EXAMPLE 22

A low-temperature buffer layer made of GaN and an undoped GaN layer were grown on an off-angled sapphire substrate **11**, and first selective growth masks **13** were formed on the resultant structure in the same manner as in Example 10 except that the stripe width was 10 μm and the stripe interval was 5 μm.

This wafer was transferred to the MOVPE apparatus, and a GaN crystal **16** doped with Si at $1\times10^{19}/cm^3$ was grown on this wafer to a thickness of 10 μm.

After an n-side cladding layer **81**, an active layer **82**, a p-side cladding layer **83**, and a p-side contact layer **84** like those in Example 20 were sequentially grown, and the resultant structure was subjected to the same processing as in Example 20, thereby obtaining a 350-μm square LED device. The output level of this LED device increased about 5% as compared with the LED device of Example 20, and the yield of the device itself was high as in Example 20.

EXAMPLE 22

Three types of Si-doped GaN crystals **16** were grown in the same manner as in Example 14 except that the stripe intervals of the respective types of crystals were set to 5 μm, 3 μm, and 1 μm.

When the number of etching pits was measured in the same manner as in Example 14, the number of etching pits with the stripe intervals being 3 μm and 1 μm was smaller than that with the stripe interval being 5 μm by about 20%.

EXAMPLE 23

This example will be described with reference to FIGS. **1**A to **1**C, in particular.

A sapphire substrate **11**, 2 inches in diameter, having a C plane as a major surface and an ORF surface forming an A plane was set in the MOVPE reaction vessel. A low-temperature buffer layer made of GaN was grown on the substrate at a temperature of 500° C. by using hydrogen gas as a carrier gas and TMG and ammonia as source gases. An undoped GaN layer was then grown on the buffer layer to a thickness of 5 μm at a temperature of 1,050° C., thereby forming an underlayer **12** having a two-layer structure.

The wafer, on which this underlayer **12** was formed, was removed from the MOVPE reaction vessel, and a striped photomask was formed on the upper surface of the underlayer **12**. By using a CVD apparatus, 1-μm thick first selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval of 2 μm were formed on the wafer.

The wafer, on which the selective growth masks **13** were formed, was set in the MOVPE reaction vessel again, and an undoped GaN crystal **16** was grown on the wafer to a thickness of 30 μm at a temperature of 1,050° C. by feeding ammonia at a flow rate of 0.27 mol/min and TMG at a flow rate of 225 micromol/min (V/III ratio=1200). After this growth step, the cross-section of the GaN crystal **16** was observed by a TEM. As a result, it was found that the number of crystal defects in a lower-side region up to a level of about 5 μm from the interface between the crystal **16** and the underlayer **12** was large ($10^8/cm^2$ or more), and a region above this lower-side region had a small number of crystal defects ($10^6/cm^2$ or less) and could be satisfactorily used as a nitride semiconductor crystal substrate. Relatively many crystal defects were present in the portions, of the upper surface of the crystal **16** after the growth step, which correspond to the middle portions of the respective stripe masks and the middle portions of the window portions. However, the number of crystal defects in these portions was smaller than that in the case of V/III ratio of 2,000 or more by 100 times or more.

An n-side buffer layer **211** made of GaN doped with Si at $3\times10^{18}/cm^3$ was grown on the GaN crystal **16** to a thickness of 5 μm by using ammonia as a source gas and silane gas as a dopant gas.

A crack prevention layer **212** made of $In_{0.06}Ga_{0.94}N$ was grown on the n-side buffer layer **211** at a temperature of 8000 by using TMG, TMI, and ammonia as source gases.

Subsequently, 25-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{19}/cm^3$ (using TMA, TMG, ammonia, and silane gas) and 25-angstroms thick second layers made of undoped GaN (using TMG and ammonia) were alternately grown at 1,050° C. to form an n-side cladding layer **213** having a total thickness of 0.3 μm and a superlattice structure.

An n-side light guide layer **214** made of undoped GaN was grown to a thickness of 0.1 μm at 1,050° C.

Subsequently, 40-angstroms thick well layers made of undoped $In_{0.2}Ga_{0.8}N$ and 100-angstroms thick barrier layers made of undoped $In_{0.01}Ga_{0.95}N$ were alternately stacked at a temperature of 800° C. by using TMG, TMI, and. ammonia to grow an active layer **215** having a barrier layer as the last layer, a total thickness of 440 angstroms, and a multi quantum well structure.

The temperature was then raised to 1,050° C., and a p-side cap layer **216** made of p-type $Al_{0.3}Ga_{0.7}N$ doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of a p-side light guide layer **217** was grown to a thickness of 300 angstroms by using TMG, TMA, ammonia, and Cp_2Mg.

The p-side light guide layer **217** made of undoped GaN and having a band gap energy lower than that of the p-side cap layer **216** was grown to a thickness of 0.1 μm at 1,050° C. by using TMG and ammonia.

Subsequently, 25-angstroms thick first layers made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$ and 25-angstroms thick second layers made of undoped GaN were alternately stacked at 1,050° C. to grow a p-side cladding layer **218** having a total thickness of 0.8 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $2\times10^{20}/cm^3$ was grown on the p-side cladding layer **218** to a thickness of 150 angstroms at 1,050° C.

The wafer, on which the nitride semiconductor layers were grown in the above manner, was annealed in a nitrogen atmosphere at 700° C. to further decrease the resistances of the layers doped with a p-type impurity.

After the annealing step, the wafer was removed from the reaction vessel, and the p-side contact layer **219** as the

uppermost layer and the p-side cladding layer **218** were etched to provide a ridge having a stripe width of 4 μm by using the RIE apparatus. At this time, ridge stripes were formed in surface regions other than regions at positions corresponding to the middle portions of the stripe masks **13** and the middle portions of the windows in which crystal defects appeared. The formation of ridge stripes at positions where almost no crystal defects are present tends to make it difficult to cause dislocation of crystal defects from the substrate to the active region during laser oscillation. This prolongs the service life of the device and improves the reliability, resulting in an improvement in reliability.

A protective mask was formed on the ridge top surface and etched by RIE to expose the upper surface of the n-side buffer layer **211**. This exposed n-side buffer layer **211** also serves as a contact layer for the formation of n-side electrodes **223***a* and **223***b*. Note that etching can be performed up to the region, of the GaN crystal **16**, in which many crystal defects are present, and the exposed surface can be provided as a contact layer.

A p-side electrode **220** made of Ni and Au was formed, in the form of a stripe, on the top surface of the p-side contact layer **219** forming the ridge. The n-side electrodes **223***a* and **223***b* made of Ti and Al were formed, in the form of stripes, on the surface portions, of the n-side buffer layer **211**, which were exposed by the above etching.

After this step, an insulating film **221** made of SiO_2 was formed on the side surfaces, of the nitride semiconductor layer, which were exposed by the above etching, and a p-pad electrode **222** electrically connected to the p-electrode **220** through the insulating film **221** was formed.

The obtained wafer was transferred to the polishing apparatus to lap the lower surface of the sapphire substrate **11** to a thickness of 70 μm by using a diamond abrasive. Thereafter, the lower surface of the sapphire substrate **11** was polished by 1 μm into a mirror surface by using a finer abrasive. The entire lower surface was metallized with Au/Sn.

After this step, the wafer was scribed on the Au/Sn side to be cleaved in the form of a bar in a direction perpendicular to the striped electrodes, thereby forming a cleavage surface. A dielectric multilayer film made of SiO_2 and TiO_2 was formed on the resonance surface. Finally, the bar was cut in a direction parallel to the p-electrode to obtain an LD device chip. This chip was placed on the heat sink with the chip facing up, and the respective electrodes were bonded to each other by wire bonding. When this LD device was laser-oscillated at room temperature, continuous oscillation of an oscillation wavelength of 405 nm was observed at a threshold current density of 2.0 kA/cm^2 and a threshold voltage of 4.0V. The device exhibited a life of 1,000 hrs or more. In addition, 500 LD devices were arbitrarily extracted selected from the LD devices obtained from the above wafer, and the service lives of the 500 LD devices were measured to find that 70% or more of the devices exhibited service lives of 10,000 hrs or more.

The LD devices were manufactured in the same manner as in Example 23 except that the undoped GaNGaN crystals **16** were grown to a thickness of 30 μm by setting the flow rate of ammonia to 0.36 mol/min and the flow rate of TMG to 162 micromol/min (V/III ratio=2222), and the ridge stripes were formed at arbitrary positions. Of the 500 LD devices arbitrarily selected from the obtained LD devices, 5% or less achieved service lives of 10,000 hrs or more.

EXAMPLE 24

LD devices were manufactured by the same method as in Example 23 except that each GaN crystal **16** was grown to a thickness of 10 μm. In this case, the number of crystal defects in the surface of the GaN crystal **16** tended to be larger than that in the LD device of Example 23 on about one order of magnitude. In addition, of 500 LD devices arbitrarily selected from the obtained LD devices, 5% or more achieved service lives of 10,000 hrs or more.

EXAMPLE 25

This example will be described with reference to FIG. **11** mainly.

An Si-doped GaN crystal was grown to a thickness of 30 μm in the same manner as in Example 23 except that the GaN crystal **16** was grown by feeding ammonia at 0.27 mol/min and TMG at 150 micromol/min (V/III ratio=1800) and adding silane gas to these source gases. In this GaN crystal **16**, the number of crystal defects in a lower-side region up to a level of about 5 μm from the interface between the crystal **16** and an underlayer **12** was large, and a region above this lower-side region had a small number of crystal defects (10^6/cm^2 or less) and could be satisfactorily used as a nitride semiconductor crystal substrate.

Subsequently, nitride semiconductor layers **211** to **219** identical to those in Example 23 were formed. In this case, an LD device was obtained in the same manner as in Example 23 except that a portion of the GaN crystal **16** was removed up to a depth of about 6 μm from the upper surface by etching to expose the GaN crystal **16** in a region having relatively many crystal defects, and n-side electrodes **223***a* and **223***b* were formed on the exposed surfaces. Similar to the LD device of Example 23, this LD device continuously oscillated with a low threshold. Of 500 LD devices, 50% or more achieved service lives of 10,000 hrs or more.

EXAMPLE 26

LD devices were manufactured by the same method as in Example 23 except that each GaN crystal **16** was grown by setting the flow rate of ammonia to 0.26 mol/min and the flow rate of TMG to 180 micromol/min (V/III ratio=1500). As a result, almost the same number of LD devices as that in Example 23 could be obtained, which continuously oscillated with a low threshold.

EXAMPLE 27

LD devices were manufactured by the same method as in Example 23 except that in growing each GaN crystal, the flow rate of TMG was increased to set the V/III ratio to 800. As a result, almost the same number of LD devices as that in Example 23 could be obtained, which continuously oscillated with a low threshold.

EXAMPLE 28

LD devices were manufactured by the same method as in Example 23 except that in growing each GaN crystal **16**, the flow rate of ammonia was set to 0.15 mol/min and the flow rate of TMG was set to 5 millimol/min (V/III ratio=30). As a result, each LD device continuously oscillated with a low threshold. Of 500 LD devices arbitrarily selected from the obtained LD devices, 30% or more exhibited service lives of 10,000 hrs or more.

EXAMPLE 29

Nitride semiconductor layers **211** to **219** were grown in the same manner as in Example 23 except that in growing a GaN crystal **16**, an Si-doped GaN crystal was grown to a thickness of 9 μm by doping the crystal with Si. When the

wafer was removed from the reaction vessel, the wafer has warped due to the thermal expansion coefficient difference between a sapphire substrate **11** and the Si-doped GaN crystal. This wafer was polished from the sapphire substrate **11** side to remove the sapphire substrate **11**, an underlayer **12**, and selective growth masks **13**. The obtained GaN crystal in a free state became substantially flat without warpage.

As in Example, 23, the p-side contact layer **219** and the p-side cladding layer **218** were etched in the form of a ridge, and a p-side electrode **220** and an insulating film **221** were formed. Thereafter, a p-pad electrode **222** was formed. In this case, since the selective growth masks **13** were removed, it was difficult to match the position of each ridge stripe with a corresponding window portion by microscopic observation. N-side electrodes **223***a* and **223***b* made of Ti/Al were formed on almost the entire exposed lower surface, of the GaN crystal **16**, in which many crystal defects were present. Thereafter, this structure was processed in the same manner as in Example 23 to obtain LD devices. These LD devices also continuously oscillated at room temperature with a low threshold. Of arbitrarily selected 500 LD devices, 70% or more exhibited service lives of 10,000 hrs or more.

EXAMPLE 30

This example will be described with reference to FIGS. 1A to 1C and 5A and 5B.

A sapphire substrate **11**, 2 inches in diameter, having a C plane as a major surface and an ORF surface forming an A plane was set in the MOVPE reaction vessel, and a low-temperature buffer layer made of GaN was grown on the substrate to a thickness of 200 angstroms at a temperature of 500° C. by using hydrogen gas as a carrier gas and TMG and ammonia as source gases. An undoped GaN layer was grown on the buffer layer to a thickness of 4 μm at a temperature of 1,050° C. to form an underlayer **12** having a two-layer structure.

The wafer, on which this underlayer **12** was formed, was removed from the MOVPE reaction vessel, and a striped photomask was formed on the upper surface of the underlayer **12**. Then, 0.5-μm thick first selective growth masks **13** made up of many SiO_2 stripes having a stripe width of 10 μm and a stripe interval of 2 μm were formed on the wafer by using the CVD apparatus.

The wafer, on which the selective growth masks **13** were formed, was set in the MOVPE reaction vessel again, and an undoped GaN crystal **16** was grown on the wafer to a thickness of 30 μm at a temperature of 1,050° C. by feeding ammonia at a flow rate of 0.27 mol/min and TMG at a flow rate of 225 micromol/min (V/III ratio=1200). When a GaN crystal is grown while the V/III molar ratio is set to 2,000 or less, the GaN crystal **15** grows laterally on the mask **13** while the grown end face is forming a facet almost perpendicular to the plane of the mask **13**. Therefore, the crystal **16** having very few crystal defects can be obtained. The grown GaN crystal (MOVPE GaN crystal) **16** has a uniform surface. When this surface region was observed with a TEM, crystal defects extending from windows **14** stopped halfway in the GaN crystal **16**, and almost no crystal defects appeared on the surface.

The wafer, on which the GaN crystal **16** was grown, was transferred to the HVPE apparatus, and an undoped GaN crystal **17** (HVPE GaN crystal) was grown on the wafer to a thickness of 200 μm by using Ga metal, HCl gas, and ammonia as raw materials. When the number of crystal defects in the surface region of the obtained HVPE GaN crystal **17** was measured by two-dimensional TEM observation, it was found that the number of crystal defect was $1\times10^4/cm^2$ or less, and hence a GaN crystal having excellent crystallinity was obtained. Very few existing crystal defects were only crystal defects extending in a direction almost parallel to the plane.

The wafer, on which HVPE GaN crystal **17** was grown, was transferred to the polishing apparatus, and the sapphire substrate **11**, the underlayer **12**, the selective growth masks **13**, and the MOVPE GaN crystal **16** were removed by using a diamond abrasive to expose the lower surface of the HVPE GaN crystal **17**, thereby obtaining Ea GaN crystal substrate in a free state which has a total. thickness of 195 μm. Note that the number of crystal defects in the lower surface of this crystal substrate was as small as $1\times10^5/cm^2$ or less.

EXAMPLE 31

A GaN crystal substrate in a free state was obtained by the same method as in Example 30 except that in growing an HVPE GaN crystal **17**, silane gas was added to source gases, GaN was grown first while it was doped with Si at $1\times10^{19}/cm^3$, the flow rate of silane gas was decreased with the growth of GaN, and the GaN crystal was finally grown as GaN doped with Si at $5\times10^{16}/cm^3$, thereby growing 200-μm thick GaN having an Si concentration gradient. In this GaN crystal substrate, the number of crystal defects in the surface with a small amount of Si was almost equal to that in the crystal substrate in Example 3.

EXAMPLE 32

An MOVPE GaN crystal **16** was obtained by the same method as in Example 30 except that in growing the MOVPE GaN crystal **16**, silane gas was added to source gases, GaN was grown first while it was doped with Si at $1\times10^{19}/cm^3$, the flow rate of silane gas was decreased with the growth of GaN, and the GaN crystal was finally grown as GaN doped with Si at $1\times10^{17}/cm^3$, thereby growing 20-μm thick GaN having an Si concentration gradient. An Si-doped HVPE GaN crystal **17** was grown to a thickness of 200 μm by the same method as in Example 30 except that in growing the HVPE GaN crystal, GaN was doped with Si at $1\times10^{17}/cm^3$. Thereafter, a sapphire substrate **11**, an underlayer **12**, and selective growth masks **13** were all removed, and the MOVPE GaN crystal was removed by a thickness of 15 μm.

In the GaN crystal substrate having the two-layer structure made up of the MOVPE GaN crystal and the HVPE GaN crystal obtained in the above manner, the number of crystal defects in the major surface of the HVPE GaN crystal was almost equal to that in the GaN crystal substrate in Example 30, but the number of crystal defects in the lower surface of the MOVPE GaN crystal was larger than that in the major surface of the HVPE GaN crystal by about one order of magnitude.

EXAMPLE 33

This example will be described with reference to FIG. **12**.

An n-side contact layer **211** made of GaN doped with Si at $3\times10^{18}/cm^3$ was grown on the upper surface (on the opposite side to the lower surface from which the sapphire substrate **11** and the like were removed by polishing) of an HVPE GaN crystal substrate obtained as in Example 30 to a thickness of 4 μm at 1,050° C. by using ammonia and TMG as source gases and silane gas as an impurity gas.

A crack prevention layer **212** made of $In_{0.06}Ga_{0.94}N$ was grown on the n-side contact layer **211** to a thickness of 0.15

μm at a temperature to 800° C. by using TMG, TMI, and ammonia as source gases.

Subsequently, 25-angstroms thick first layers (using TMA, TMG, and ammonia) made of undoped $Al_{0.16}Ga_{0.84}N$ and 25-angstroms thick second layers (TMG, ammonia, and silane) made of n-type GaN doped with Si at $1\times10^{19}/cm^3$ were alternately grown on the crack prevention layer **212** at 1,050° C. to grow an n-side cladding layer **213** having a total thickness of 1.2 μm and a superlattice structure.

An n-side light guide layer **214** made of undoped GaN was grown on the n-side cladding layer **213** to a thickness of 0.1 μm at 1,050° C. by using TMG and ammonia.

Subsequently, 100-angstroms thick barrier layers made of undoped $In_{0.01}Ga_{0.95}N$ and 40-angstroms thick well layers made of undoped $In_{0.2}Ga_{0.8}N$ were alternately grown three times at a temperature of 800° C. to grow an active layer **215** having a barrier layer as the last layer, a total thickness of 520 angstroms, and an MQW structure. The temperature was then raised to 1,050° C. to grow a p-side cap layer **216** made of p-type $Al_{0.3}Ga_{0.7}N$ doped with Mg at $1\times10^{20}/cm^3$ to a thickness of 300 angstroms by using TMG, TMA, ammonia, and Cp_2Mg.

A p-side light guide layer **217** made of GaN doped with Mg at $5\times10^{16}/cm^3$ was grown on the p-side cap layer **216** to a thickness of 0.1 μm.

Subsequently, 25-angstroms thick first layers made of undoped $Al_{0.16}Ga_{0.84}N$ and 25-angstroms thick second layers made of GaN doped with Mg at $1\times10^{19}/cm^3$ were alternately grown to grow a p-side cladding layer **218** having a total thickness of 0.6 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ was grown to a thickness of 150 angstroms.

The wafer, on which the nitride semiconductor layers were grown in the above manner, was removed from the reaction vessel. An SiO_2 protective film was then formed on the upper surface of the p-side contact layer **219** as the uppermost layer, and the wafer was etched by RIE using $SiCl_4$ gas to expose the upper surface, of the n-side contact layer **211**, on which an n-side electrode was to be formed.

A mask having a predetermined shape was used for the p-side contact layer **29** as the uppermost layer, and the p-side contact layer **219** and the p-side cladding layer **218** were etched to form a ridge stripe having a width of 1 μm. Thereafter, a ZrO_2 insulating film **221** was formed on the side surfaces of the ridge and the exposed surface of the p-side cladding layer **218** such that the top portion of the p-side contact layer **219** was exposed. A p-side electrode **220** electrically connected to the p-side contact layer **219** through the insulating film **221** was formed. An n-side electrode **223** was formed on the surface, of the n-side contact layer **211**, which was exposed by etching.

After the GaN crystal substrate **1000** of the wafer obtained in the above manner was thinned by polishing, the GaN crystal substrate **1000** was cleaved to form a resonance surface of an LD device on the cleavage surface. After cleavage, each LD device was separated as a chip, and the lower surface of the GaN crystal substrate **1000** was placed on the heat sink. This LD device exhibited continuous laser oscillation at room temperature at a threshold current density of 1.5 kA/cm^2, and a service life of 1,000 hrs or more with an output of 20 mW.

In this example, the LD device was manufactured by using the substrate obtained as in Example 30. However, even in a structure for extracting both n- and p-electrodes from the same surface side, a nitride semiconductor substrate doped with an n-type impurity with a concentration gradient, obtained as in Examples 31 and 32, can be used. In this case, the n-side contact layer **211** is not required, and the n-side electrode **223** can be formed on the surface, of an MOVPE or HVPE crystal with a concentration gradient, which is exposed by etching.

EXAMPLE 34

A crack prevention layer **212**, an n-side cladding layer **213**, an n-side light guide layer **214**, an active layer **215**, a p-side cap layer **216**, a p-side light guide layer **217**, a p-side cladding layer **218**, and a p-side contact layer **219** were sequentially grown on the upper surface (on the opposite side to the lower surface from which the sapphire substrate **11** and the like were removed) of an HVPE crystal doped with Si with a concentration gradient, which was obtained as in Example 31, in the same manner as in Example 33 without forming the n-side contact layer **211**.

As in Example 33, the p-side contact layer **219** and the p-side cladding layer **218** were etched to form a ridge stripe having a width of 1 μm, an insulating film **221** was formed, and a p-side electrode **220** was formed on the p-side contact layer. An n-side electrode **223** was formed on the lower surface of the GaN crystal substrate. Thereafter, the GaN crystal substrate was polished to a thickness that allows cleavage from the lower surface, and the substrate was cleaved in the same manner as in Example 33, thereby obtaining an LD device. In this example, even if the GaN crystal substrate was polished, since a concentration gradient was set, the exposed surface of the nitride semiconductor substrate was always a surface heavily doped with an n-type impurity. The obtained LD device had substantially the same characteristics as those of Example 33.

EXAMPLE 35

This example will be described with reference to FIGS. 7A to 7D.

A sapphire substrate 11 having a C plane as a major surface and an ORF surface as an A plane was set in the MOVPE reaction vessel. A low-temperature buffer layer **12** made of GaN was then grown on the sapphire substrate **11** to a thickness of about 200 angstroms at a temperature of 510° C. by using hydrogen as a carrier gas and ammonia and TMG as source gases. A GaN layer **71** doped with Si at $1\times10^{18}/cm^3$ was grown on the underlayer **12** to a thickness of 2 μm at a temperature of 1,050° C. by using TMG and ammonia as source gases.

After this step, a striped photomask was formed on the GaN layer **71**, and 1-m thick silicon dioxide stripes having a stripe width of 15 μm and a stripe interval of 3 μm were formed by using the sputtering apparatus. The GaN layer **71** was etched halfway to form grooves **72** by using the RIE apparatus. The GaN layer 71 was exposed only at the side surfaces and bottom surfaces of the grooves **72**. Note that each silicon dioxide stripes extended in a direction perpendicular to the ORF surface of the sapphire substrate **11**.

After the grooves 72 were formed in this manner, a. second silicon dioxide layer was formed on the entire surface of the resultant structure, including the first silicon dioxide masks and the side and bottom surfaces of the grooves 72. Thereafter, only the portions, of the second silicon dioxide layer, which were located above the side surfaces of the grooves **72** were etched, except for the portions above the bottom surfaces of the grooves **72** and the silicon dioxide stripes, by using a gas mixture of CF_4 and O_2

gases. As a result, first growth control masks **73** made of the first and second silicon dioxides were formed the walls between the adjacent grooves **72**, and second growth control masks **74** made of the second silicon dioxide were formed on the bottom portions of the grooves **73**.

The wafer, on which the GaN layer **71**, the grooves **72**, and the first and second growth control masks **73** and **74** were formed, was set in the MOVPE reaction vessel. A GaN crystal **76** doped with Si at $1\times10^{18}/cm^3$ was grown on the wafer to a thickness of 30 μm at 1,050° C. by using TMG and ammonia as source gases and silane gas as a dopant gas.

The wafer, on which the Si-doped GaN crystal **76** was grown, was removed from the reaction vessel.

For comparison, the buffer layer **12** was grown on the sapphire substrate **11**, and the GaN layer **71** was grown on the buffer layer to a thickness of 30 μm to obtain a comparative GaN substrate.

When the numbers of crystal defects in the two GaN substrates were measured by two-dimensional TEM observation, it was found that the number of crystal defects in the GaN substrate in Example 35 was $6\times10^{6}/cm^2$, whereas that in the comparative GaN substrate was $1\times10^{10}/cm^2$.

EXAMPLE 36

An underlayer **12** and an Si-doped GaN layer **71** were grown on a sapphire substrate **11** by the same method as in Example 35. Grooves **72** similar to those in Example 35 were formed in the GaN layer **71** by dicing. A silicon dioxide layer was formed on the entire surface of the resultant structure. Only the portions, of the silicon dioxide layer, which were located on the side surfaces of the grooves **72** were removed by etching to form first growth control masks **73** covering the top surfaces of the walls between the grooves **72** and second growth control masks **74** covering the bottom portions of the grooves **72**. The GaN layer **71** was exposed only at the side surfaces of the grooves **72**. An Si-doped GaN crystal **76** was grown on this wafer by the same method as in Example 35. When the number of crystal defects in the obtained GaN crystal substrate **76** was measured, a good result was obtained as in Example 35.

EXAMPLE 37

An Si-doped GaN crystal **76** was grown by the same method as in Example 35 except that a GaN layer **71** was etched up to a sapphire substrate **11**. This GaN crystal had few crystal defects like the crystal in Example 35.

EXAMPLE 38

This example will be described with reference to FIGS. **8**A and **8**C.

An Si-doped GaN crystal **76** was grown to a thickness of 200 μm by the same method as in Example 35. A sapphire substrate **11**, an underlayer **12**, a GaN layer **71**, and growth control masks **73** and **74** were removed from this wafer by polishing to obtain an Si-doped GaN crystal substrate in a free state.

This Si-doped GaN crystal substrate (substrate **1000**) was set in the MOVPE reaction vessel of the MOVPE apparatus, and a high-temperature buffer layer **81** made of GaN doped with Si at $1\times10^{18}/cm^3$ was grown on the upper surface of the substrate at 1,050° C.

Subsequently, a 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer **82** having a single quantum well structure, a 0.3-angstroms thick p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$, and a 0.5-μm thick p-side contact layer **84** made of GaN doped with Mg at $1\times10^{20}/cm^3$ were sequentially grown on this high-temperature buffer layer **81**.

The wafer, on which the nitride semiconductor layers were formed in this manner, was removed from the reaction vessel and was annealed in a nitrogen atmosphere at 600° C. to decrease the resistances of the p-side cladding layer **83** and the p-side contact layer **84**. Thereafter, etching was performed form the p-side contact layer **84** side to expose the upper surface of the GaN crystal substrate **1000**.

After the etching step, a 200-angstroms thick light-transmitting p-electrode **85** made of Ni/Au was formed on almost the entire upper surface of the p-side contact layer **84**. A 0.5-μm thick pad electrode **86** for bonding was formed on the p-electrode **35**.

Subsequently, a 0.5-μm thick n-side electrode **87** was formed on the entire lower surface of the GaN crystal substrate **1000**.

The obtained wafer was scribed from the n-electrode **87** side to cleave the M plane ($(1\bar{1}00)$ plane) of the GaN substrate **1000** along a surface perpendicular to the M plane, thereby obtaining a 300-μm square LED chip. This LED emitted 520-nm green light with 20 mA. The output level and electrostatic breakdown voltage of the LED were twice or more those of a device obtained by growing a nitride semiconductor device structure on a conventional sapphire substrate. That is, this device exhibited excellent characteristics.

EXAMPLE 39

This example will be described with reference to FIG. **10**.

An Si-doped GaN crystal **76** was grown to a thickness of 200 μm by the same method as in Example 35. A sapphire substrate **11**, an underlayer **12**, a GaN layer **71**, and growth control masks **73** and **74** were removed from this wafer by polishing to obtain an Si-doped GaN crystal substrate in a free state.

This Si-doped GaN crystal substrate (substrate **1000**) was set in the MOVPE reaction vessel of the MOVPE apparatus. A total of 100 20-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{19}/cm^3$ and 20-angstroms thick second layers made of undoped GaN were alternately grown on the upper surface of the Si-doped GaN crystal substrate **1000** without forming a buffer layer **211** and a crack prevention layer **212** to form an n-side cladding layer **213** having a total thickness of 0.4 μm and a superlattice structure.

An n-side light guide layer **214** made of n-type GaN doped with Si at $1\times10^{17}/cm^3$ was grown on the n-side cladding layer **213** to a thickness of 0.1 μm.

Subsequently, 25-angstroms thick well layers made of $In_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{17}/cm^3$ and 50-angstroms thick barrier layers made of $In_{0.01}Ga_{0.95}N$ doped with Si at $1\times10^{17}/cm^3$ were alternately grown to form an active layer **215** having a total thickness of 175 angstroms and a multi quantum well (MQW) structure.

A p-side cap layer **216** made of p-type $Al_{0.3}Ga_{0.9}N$ doped with Mg at $1\times10^{20}/cm^3$ and having a band gap energy higher than that of a p-side light guide layer **217** and that of the active layer **215** was grown to a thickness of 300 angstroms.

The p-side light guide layer **217** made of p-type GaN doped with Mg at $1\times10^{18}/cm^3$ and having a band gap energy lower than that of the p-side cap layer **216** was grown to a thickness of 0.1 μm.

After this step, 20-angstroms thick first layers made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$ and

20-angstroms thick second layers made of p-type GaN doped with Mg at $1\times10^{20}/cm^3$ were alternately grown to form a p-side cladding layer **218** having a total thickness of 0.4 μm and a superlattice structure.

Finally, a p-side contact layer **219** made of p-type GaN doped with Mg at $2\times10^{20}/cm^3$ was grown to a thickness of 150 angstroms.

The wafer, on which the nitride semiconductor layers were formed, was annealed in a nitrogen atmosphere at 700° C. to decrease the resistance of each p-side layer in the reaction vessel. After the annealing step, the wafer was removed from the reaction vessel, and the p-side contact layer **219** as the uppermost layer and the p-side cladding layer **218** were etched by the RIE apparatus to obtain a ridge having a stripe with of 4 μm. A p-side electrode **220** made of Ni/Au was then formed on the entire top surface of the ridge. An SiO_2 insulating film **221** was formed on the exposed surfaces of a p-side cladding layer **48** and a contact layer **49** except for the p-electrode **220**. A pad electrode **222** electrically connected to the p-electrode **220** through this insulating film **221** was formed.

After this step, a 0.5-μm thick n-side electrode **223** made of Ti/Al was formed on the entire lower surface of the GaN crystal substrate **1000**. A thin film made of Au/Sn and used for metallization for a heat sink was formed on the n-side electrode **223**.

Subsequently, the wafer was scribed from the n-electrode **223** to cleave the GaN substrate **1000** in the form of a bar along the M plane ((1100) plane) of the GaN crystal **1000** (the plane corresponding to a side surface of the hexagonal prism in FIG. **3**) so as to form resonance surfaces. A dielectric multilayer film made of SiO_2 and TiO_2 was formed on both or one of the resonance surfaces. Finally, the bar was cut in a direction parallel to the p-electrode to obtain a laser chip. The chip was then placed on a heat sink with the chip facing up (in a state wherein the substrate opposes the heat sink), and the pad electrode **222** was subjected to wire bonding. When the resultant LD device was laser-oscillated at room temperature, continuous oscillation of an oscillation wavelength of 405 nm was observed at a threshold current density of 2.0 kA/cm^2 and a threshold voltage of 4.0V. This device exhibited a service life of 1,000 hrs or more.

EXAMPLE 40

This example will be described with reference to FIG. **8**.

An undoped GaN crystal **76** was grown by the same method as in Example 35 except for the GaN crystal was grown without doping it with Si. This GaN crystal **76** (substrate **1000**) was used to manufacture the following device structure while the crystal was supported on a sapphire substrate **11**.

A total of 100 20-angstroms thick first layers made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si at $1\times10^{19}/cm^3$ and 20-angstroms thick second layers made of undoped GaN were alternately grown on the substrate **1000** to form an n-side cladding layer **81** having a total thickness of 0.4 μm and a superlattice structure.

A 20-angstroms thick $In_{0.4}Ga_{0.6}N$ active layer **82** having a single quantum well structure, a 0.3-μm thick p-side cladding layer **83** made of $Al_{0.2}Ga_{0.8}N$ doped with Mg at $1\times10^{20}/cm^3$, and a 0.5-μm thick p-side contact layer **84** made of GaN doped with Mg at $1\times10^{20}/cm^3$ were sequentially grown on the n-side cladding layer **81**. Etching was then performed from the p-side contact layer **84** to expose the upper surface of the n-side cladding layer **81**. An n-side electrode **87** was formed on the exposed upper surface. A light-transmitting p-side electrode **85** was formed on almost the entire surface of the p-side contact layer **84**. A pad electrode **86** for bonding was formed on the electrode **85**. Finally, the lower surface of the sapphire substrate was polished to a thickness of about 50 μm, and the polished surface was scribed to obtain a 350-μm square device.

The output level and the electrostatic breakdown voltage of the obtained LED device increased about 1.5 times those of the LED device of Example 38.

What is claimed is:

1. A nitride semiconductor growth method comprising the steps of:

(a) forming a nitride semiconductor layer on a support member including a dissimilar substrate made of a material different from a nitride semiconductor and having a major surface;

(b) forming a plurality of recess portions having bottom surfaces substantially parallel to an upper surface of the support member in said nitride semiconductor layer;

(c) selectively forming a first growth control mask on a top surface of the nitride semiconductor layer to selectively expose the nitride semiconductor layer from side surfaces of the recess portions; and

(d) growing a nitride semiconductor from an exposed surface of the nitride semiconductor layer by using a gaseous Group 3 element source and a gaseous nitrogen source.

2. A method according to claim **1**, wherein the recess portions are formed by a plurality of individual grooves spaced apart from each other and extending parallel.

3. A method according to claim **2**, wherein the plurality of individual grooves have a plurality of individual walls formed therebetween, and said first growth control mask is made up of individual stripes formed on top surfaces of the respective individual walls.

4. A method according to claim **3**, wherein a total surface area of said first growth control mask is larger than that of bottom surfaces of the grooves.

5. A method according to claim **4**, wherein a ratio of a width of each of the individual stripes to a width of each of the grooves is more than 1 and not more than 20.

6. A method according to claim **5**, wherein each of the grooves has a depth of 500 angstroms to 5 μm.

7. A method according to claim **3**, wherein the dissimilar substrate is a sapphire substrate having a major surface forming a (0001) plane, and the respective individual stripes extend in a direction perpendicular to a $(11\bar{2}0)$ plane of sapphire.

8. A method according to claim **3**, wherein the dissimilar substrate is a sapphire substrate having a major surface forming a $(11\bar{2}0)$ plane, and the respective individual stripes extend in a direction perpendicular to the $(1\bar{1}20)$ plane of sapphire.

9. A method according to claim **3**, wherein the dissimilar substrate is a spinnel substrate having a major surface forming a (111) plane, and the respective stripes extend in a direction perpendicular to the (110) plane of spinnel.

10. A method according to claim **1**, wherein the step (d) further comprises doping the nitride semiconductor portion with an n-type impurity during growth of the first nitride semiconductor portion.

11. A method according to claim **10**, wherein the n-type impurity is added such that a doping concentration decreases with an increase in distance from the dissimilar substrate.

12. A method according to claim **1**, wherein the gaseous nitrogen source and the gaseous Group 3 element source are supplied at a molar ratio not more than 2,000.

13. A method according to claim 12, wherein the gaseous nitrogen source and the gaseous Group 3 element source are supplied at a molar ratio of not less than 10.

14. A method according to claim 12, wherein growth of the nitride semiconductor portion in the step (d) is performed by a metal organic vapor-phase epitaxial method.

15. A method according to claim 14, wherein growth of the nitride semiconductor portion is performed under a reduced pressure of 50 to 400 Torr.

16. A method according to claim 1, wherein the step (c) further comprises forming a second growth control mask on the bottom surfaces of the recess portions to selectively expose the nitride semiconductor layer from side surfaces of the recess portions.

17. A method according to claim 16, wherein the recess portions are formed by a plurality of individual grooves spaced apart from each other and extending parallel.

18. A method according to claim 17, wherein the plurality of individual grooves have a plurality of individual walls formed therebetween, and said first growth control mask is made up of individual stripes formed on top surfaces of the respective individual walls.

19. A method according to claim 18, wherein a portion of the nitride semiconductor layer that is exposed from a side surface of the recess portion has a thickness of not less than 100 angstroms.

20. A method according to claim 18, wherein a portion of the nitride semiconductor layer that is exposed from a side surface of the recess portion has a thickness of 1 to 10 μm.

21. A method according to claim 18, wherein the dissimilar substrate is a sapphire substrate having a major surface forming a (0001) plane, and the respective individual stripes extend in a direction perpendicular to a $(11\bar{2}0)$ plane of sapphire.

22. A method according to claim 18, wherein the dissimilar substrate is a sapphire substrate having a major surface forming a $(11\bar{2}0)$ plane, and the respective individual stripes extend in a direction perpendicular to the $(1\bar{1}20)$ plane of sapphire.

23. A method according to claim 18, wherein the dissimilar substrate is a spinnel substrate having a major surface forming a (111) plane, and the respective stripes extend in a direction perpendicular to the (110) plane of spinnel.

24. A method according to claim 16, wherein the step (d) further comprises doping the nitride semiconductor portion with an n-type impurity during growth of the first nitride semiconductor portion.

25. A method according to claim 24, wherein the n-type impurity is added such that a doping concentration decreases with an increase in distance from the dissimilar substrate.

26. A method according to claim 16, wherein the gaseous nitrogen source and the gaseous Group 3 element source are supplied at a molar ratio of not more than 2,000.

27. A method according to claim 26, wherein the gaseous nitrogen source and the gaseous Group 3 element source are supplied at a molar ratio of not less than 10.

28. A method according to claim 27, wherein growth of the nitride semiconductor portion is performed under a reduced pressure of 50 to 400 Torr.

29. A method according to claim 26, wherein growth of the nitride semiconductor portion in the step (d) is performed by a metal organic vapor-phase epitaxial method.

30. A nitride semiconductor growth method characterized by comprising the steps of forming a nitride semiconductor on a support member including a dissimilar substrate, using said nitride semiconductor as a seed crystal to grow a new nitride semiconductor in substantially only a lateral direction while suppressing growth of the nitride semiconductor in a vertical direction, and then growing the nitride semiconductor in both the vertical and lateral directions, thereby obtaining an integral nitride semiconductor crystal on a substantially entire upper surface of the support member.

* * * * *

US006325850B1

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Beaumont et al.

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(45) **Date of Patent: Dec. 4, 2001**

(54) **METHOD FOR PRODUCING A GALLIUM NITRIDE EPITAXIAL LAYER**

(75) Inventors: **Bernard Beaumont**, Valbonne; **Pierre Gibart**, Chateauneuf de Grasse; **Jean-Claude Guillaume**, La Gaude; **Gilles Nataf**, Cagnes sur Mer; **Michel Vaille**, Antibes; **Soufien Haffouz**, Nice, all of (FR)

(73) Assignee: **Centre National de la Recherché Scientifique (CNRS)**, Paris (FR)

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PCT Pub. Date: **Apr. 29, 1999**

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(52) **U.S. Cl.** **117/95**; 117/96; 117/97; 117/952; 257/103
(58) **Field of Search** 257/103; 117/95, 117/96, 97, 952

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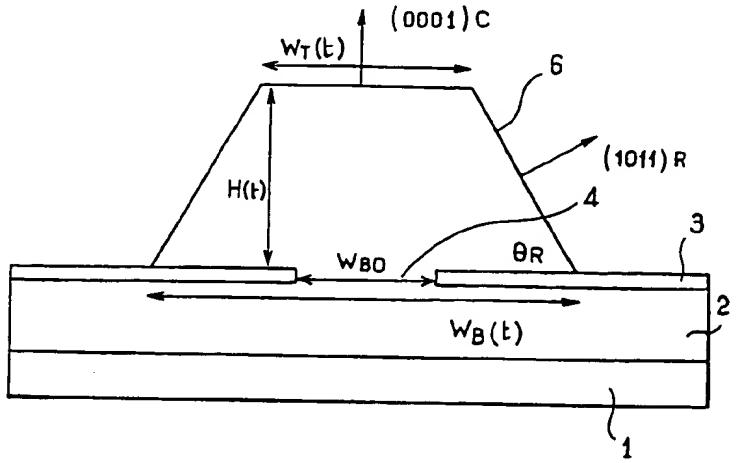
Primary Examiner—Robert Kunemund
(74) *Attorney, Agent, or Firm*—Blakely Sokoloff Taylor & Zafman

(57) **ABSTRACT**

The invention concerns a method for producing a gallium nitride (GaN) epitaxial layer characterised in that it consists in depositing on a substrate a dielectric layer acting as a mask and depositing on the masked gallium nitride, by epitaxial deposit, so as to induce the deposit of gallium nitride patterns and the anisotropic lateral growth of said patterns, the lateral growth being pursued until the different patterns coalesce. The deposit of the gallium nitride patterns can be carried out ex-situ by dielectric etching or in-situ by treating the substrate for coating it with a dielectric film whereof the thickness is of the order of one angstrom. The invention also concerns the gallium nitride layers obtained by said method.

30 Claims, 6 Drawing Sheets



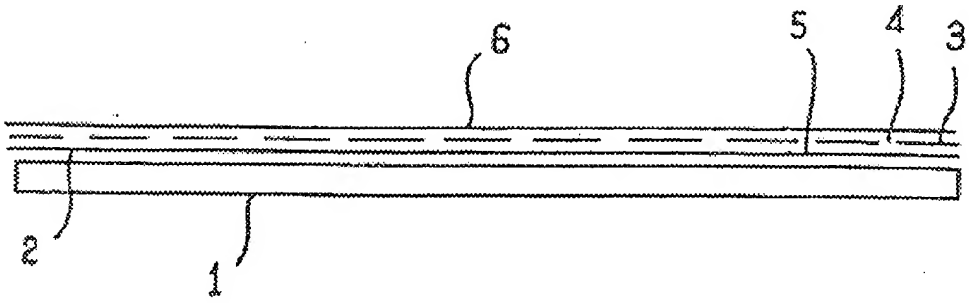


FIG_1

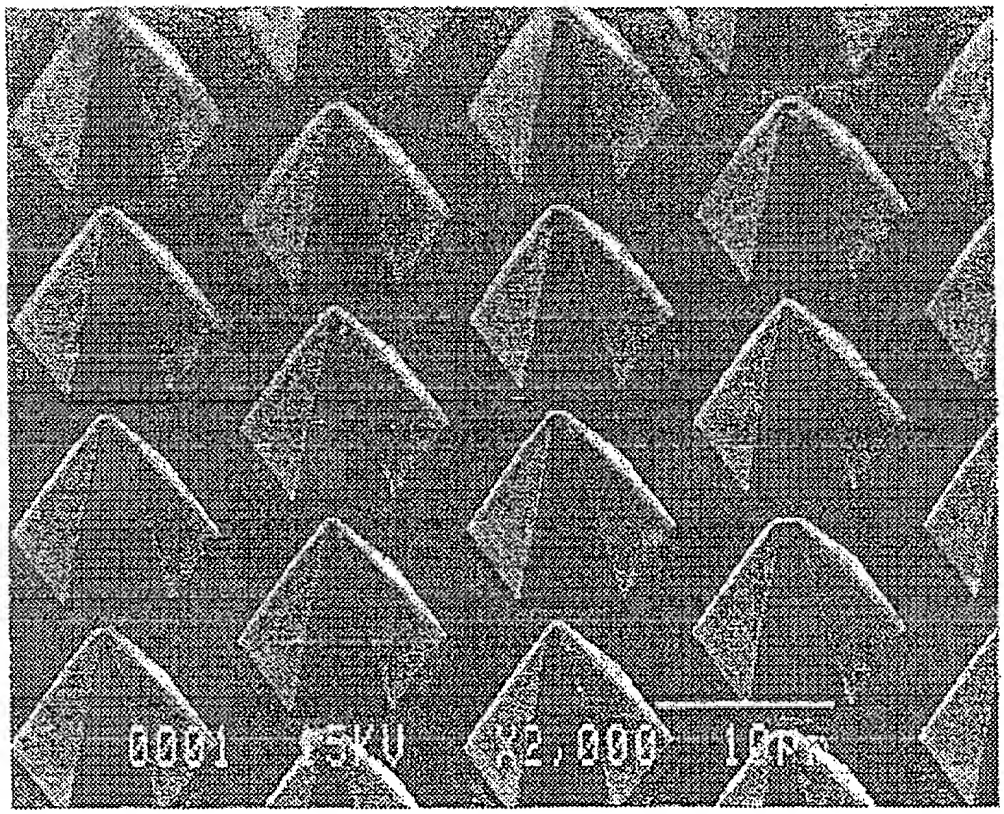


Figure 2

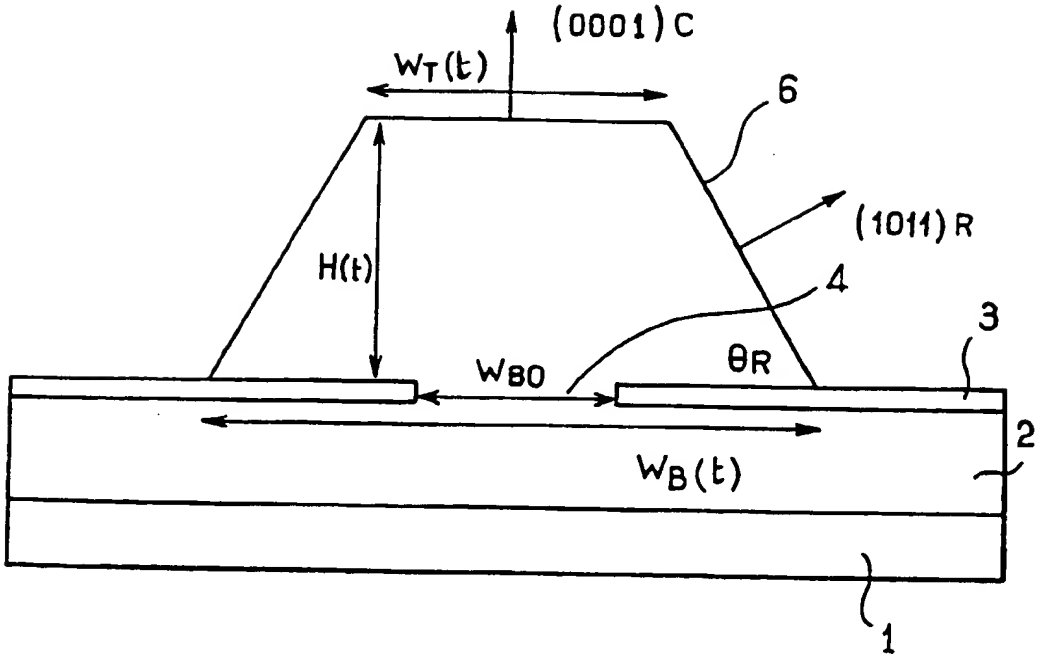


FIG_3

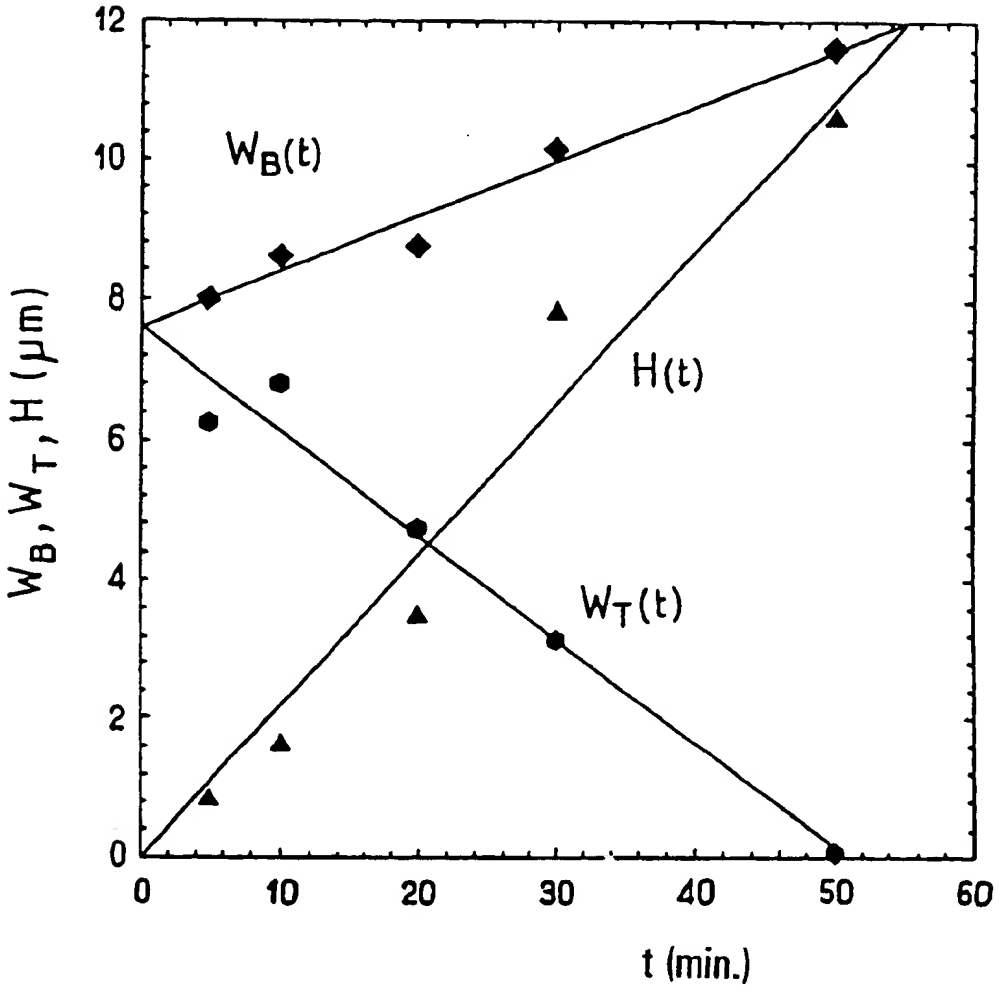


FIG. 4

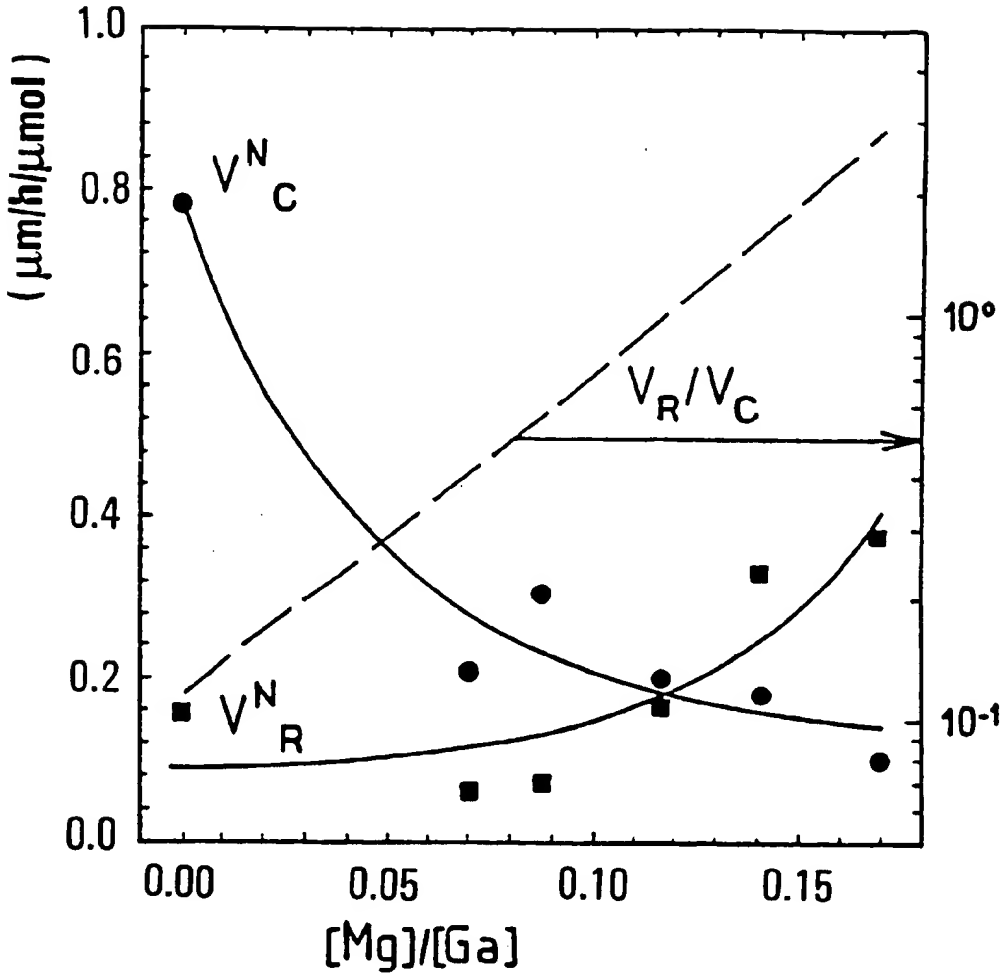

1.0
0.8
0.6
0.4
0.2
0.0
(μm/h/μmol)
V^N_C
V_R/V_C
V^N_R
10°
10^{-1}
0.00
0.05
0.10
0.15
[Mg]/[Ga]

FIG_5

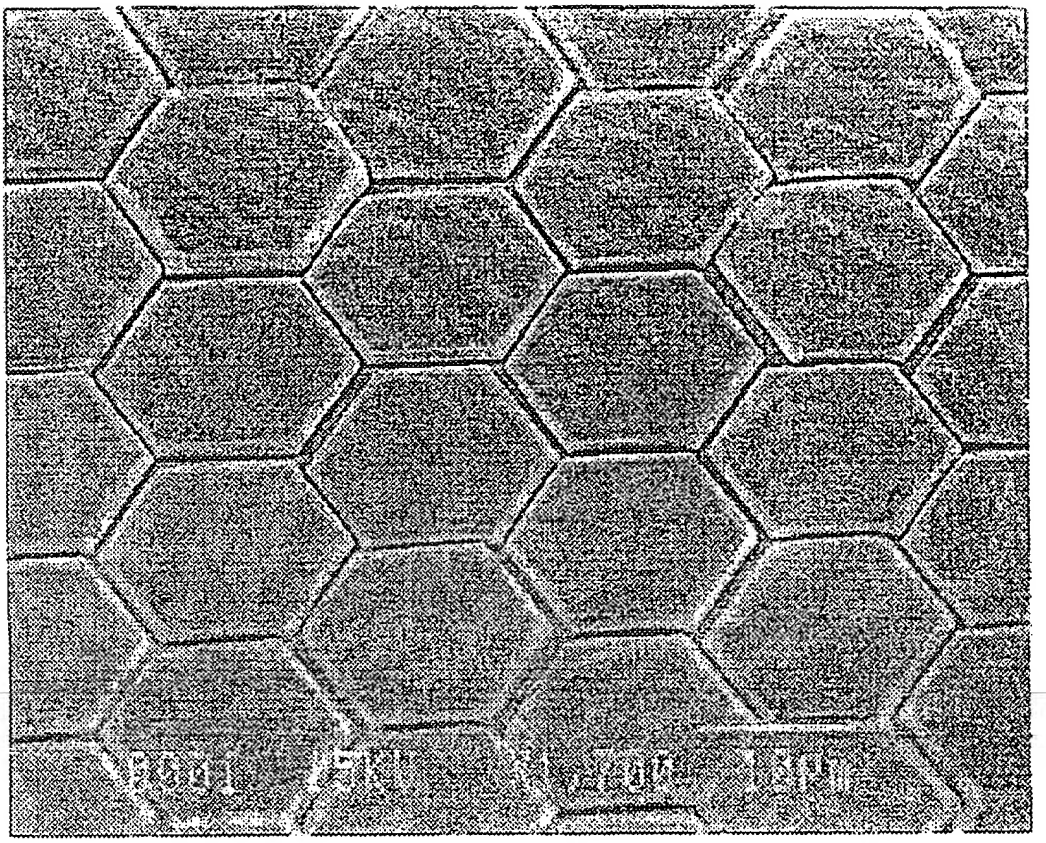


Figure 6

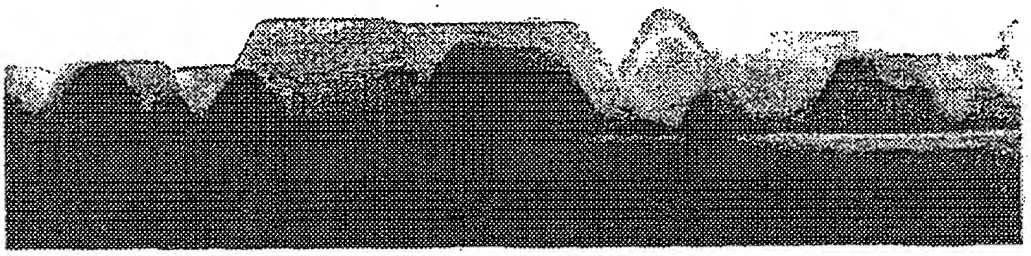


Figure 7

Figure 8

METHOD FOR PRODUCING A GALLIUM NITRIDE EPITAXIAL LAYER

The present invention relates to a process for producing an epitaxial layer of gallium nitride (GaN) as well as to the epitaxial layers of gallium nitride (GaN) which can be obtained by said process. Such a process makes it possible to obtain gallium nitride layers of excellent quality.

It also relates to the short-wavelength optical devices or the high-power high-frequency electronic devices provided with such an epitaxial gallium nitride layer.

It relates in particular to optoelectronic components formed on such gallium nitride layers.

Processes are known for obtaining relatively thick GaN layers, for example from 100 to 200 micrometers. The method commonly used is chloride and hydride vapor phase epitaxy (HVPE). Either sapphire substrates or GaN layers on sapphire 200 micrometers in thickness are used, these layers being fabricated by OrGaNoMetallic Pyrolisis Vapor Phase Epitaxy (OMVPE). However the crystal lattice parameter mismatch between sapphire and GaN is such that the build-up of stresses in the layers results in cracks and prevents the sapphire substrate from being removed. All the experimental innovations (treatment of the surface of the sapphire at the start of growth with GaCl, deposition of a ZnO interlayer) have not made it possible to solve this problem. At the present time, the relatively thick GaN layers have a double X-ray diffraction (DXD) line width of the order of at best 300 arcsec, which means that the crystallographic quality does not exceed that of the layers formed by OMVPE or by molecular beam epitaxy (MBE).

In other words, no potential sapphire, ZnO, 6H—SiC or $LiAlO_2$ substrate is ideal for nitride epitaxy (excessively high lattice mismatch and thermal expansion coefficient mismatch, thermal instability).

Moreover, the lasing effect (by optical pumping) on GaN has been known for a long time. Although diode lasers based on III–V nitride have been produced, the crystal quality of the nitride layers constituting the structure of these lasers is very average. Dislocation densities ranging from 10^9 to 10^{10} cm^{-2} have been measured.

In fact, the defects associated with the formation of relatively thick epitaxially grown GaN layers indicated above have considerably slowed down the development of diode lasers provided with such layers: high residual n, absence of single crystals and of suitable substrates, impossibility of producing p-doping.

The publication by D. Kalponek et al., Journal of Crystal Growth, 170 (1997) 340–343 mentions the localized nitride growth in apertures formed in a mask so as to form pyramidal structures. However, this document neither describes nor suggests the formation, by coalescence, of features or islands of smooth gallium nitride layers.

The publication Y. Kato, S. Kitamura, K. Hiramatsu and N. Sawaki, J. Cryst. Growth, 144, 133 (1994) describes the selective growth of gallium nitride by OMVPE on sapphire substrates on which has been deposited a thin gallium nitride layer masked by an SiO_2 layer etched so as to reveal continuous bands of gallium nitride.

However, the localized epitaxy thus carried out involves neither the lateral growth nor the growth anisotropy as will be described below.

The document EP 0,506,146 describes a process for local and lateral growth using a mask, shaped by lithography, to localize the growth. The examples of smooth layers relate in no case to gallium nitride. These examples mention GaAs homoepitaxy on a GaAs substrate and InP homoepitaxy on an InP substrate.

The object of the process according to the invention is to obtain crystalline layers allowing the production of opto-electronic devices (especially diode lasers) having life times and performance characteristics which are superior to those obtained previously.

SUMMARY OF INVENTION

The inventors have found that the treatment of a substrate by deposition of a suitable dielectric followed by deposition of gallium nitride, which is itself followed by thermal annealing, causes the formation of gallium nitride islands which are virtually defect-free.

The coalescence of such islands caused by the heat treatment results in a gallium nitride layer of excellent quality.

The invention relates firstly to a process for producing a layer of gallium nitride (GaN), characterized in that it comprises the deposition on a substrate of a dielectric layer functioning as a mask and the regrowth of gallium nitride on the masked substrate under epitaxial deposition conditions so as to induce the deposition of gallium nitride features and the anisotropic and lateral growth of said features, the lateral growth being continued until coalescence of the various features. The term "islands" instead of "features" may also be employed.

The substrate generally has a thickness of a few hundred micrometers (in particular, approximately 200 micrometers) and may be chosen from the group consisting of sapphire, ZnO, 6H—SiC, $LiAlO_2$, $LiGaO_2$ and $MgAl_2O_4$. The substrate is preferably treated beforehand by nitriding.

Preferably, the dielectric is of the Si_xN_y type, especially Si_3N_4. SiO_2 may also be mentioned, but other well-known dielectrics could be used. The deposition of the dielectric is carried out in the gallium nitride growth chamber from silane and ammonia.

Preferably, the carrier gas is an N_2/H_2 mixture.

According to a first embodiment, the dielectric layer is an atomic monolayer, or a cover of the order of the atomic plane.

Next, epitaxial regrowth on the substrate is carried out using OMVPE. Regular features or islands develop. Examination in a high-resolution electron microscope shows that the GaN dislocation density in the regular features or islands, which has therefore grown without heteroepitaxial strains, is very much less than that produced by the direct deposition of gallium nitride on the substrate. Thus, the GaN growth, which takes place laterally in the $[10\bar{1}0]$ directions on a dielectric surface, and therefore without being in epitaxial relationship with the sapphire substrate, results in much better GaN crystal quality than the usual processes. After said features have been obtained, the growth may be continued, either using OMVPE or HVPE. Growth takes place laterally, until coalescence of the islands. These surfaces resulting from the coalescence of islands exhibit crystal quality superior to the layers grown heteroepitaxially on sapphire.

The gallium nitride deposition is generally carried out in two steps. A first step, at a temperature of approximately 600° C. for the deposition of a buffer layer, from which the GaN features will emerge, then at a higher temperature (approximately 1000–1100° C.) for the growth of an epilayer from said features.

According to a second embodiment, the invention relates to a process characterized in that the dielectric layer is etched, so as to define apertures and to expose the facing

regions of the substrate, and gallium nitride is regrown under epitaxial deposition conditions on the masked and etched substrate so as to induce the deposition of gallium nitride features on the facing regions and the anisotropic and lateral growth of said features, the lateral growth being continued until coalescence of the various features.

According to a third embodiment, the invention relates to a process for producing an epitaxial layer of gallium nitride (GaN), comprising the deposition of a thin gallium nitride layer on a substrate characterized in that:

a dielectric layer is deposited on said thin gallium nitride layer;

the dielectric layer is etched so as to define apertures and to expose those regions of said thin gallium nitride layer which face them;

gallium nitride is regrown under epitaxial deposition conditions on the expitaxially grown, masked and etched substrate so as to induce the deposition of gallium nitride features on the facing regions and the anisotropic and lateral growth of said features, the lateral growth being continued until coalescence of the various features.

The process according to the invention is noteworthy in that it limits the density of defects generated by the parameter mismatch between GaN and the substrate using a method which combines localized epitaxy, growth anisotropy and lateral growth, thereby limiting the epitaxial strains.

The process according to the invention makes use of deposition and etching techniques well-known to those skilled in the art.

According to the second embodiment, a dielectric a few nanometers in thickness is deposited in the growth chamber. Next, by photolithography, apertures are defined in the dielectric layer, thus exposing micrometric regions of the surface of the substrate.

Regrowth on the masked and etched substrate is carried out using OMVPE.

The substrate generally has a thickness of a few hundred micrometers (in particular, approximately 200 micrometers) and may be chosen from the group consisting of sapphire, ZnO, 6H—SiC, $LiAlO_2$, $LiGaO_2$ and $MgAl_2O_4$.

Preferably, the dielectric is of the Si_xN_y type, especially Si_3N_4. SiO_2 may also be mentioned, but other well-known dielectrics could be used. The dielectric is deposited in the gallium nitride growth chamber from silane and ammonia directly on the substrate, as described above.

According to the third embodiment, the gallium nitride is firstly grown epitaxially on the substrate by OMVPE. The deposition of a dielectric a few nanometers in thickness is then carried out in the growth chamber. Next, by photolithography, apertures are defined in the dielectric layer, thus exposing micrometric regions of the gallium nitride surface.

Regrowth on the epitaxially grown, masked and etched substrate is carried out using OMVPE.

The substrate generally has a thickness of a few hundred micrometers (in particular, approximately 200 micrometers) and may be chosen from the group consisting of sapphire, ZnO, 6H—SiC, $LiAlO_2$, $LiGaO_2$ and $MgAl_2O_4$.

Preferably, the dielectric is of the Si_xN_y type, especially Si_3N_4. SiO_2 may also be mentioned, but other well-known dielectrics could be used. The dielectric is deposited in the gallium nitride growth chamber from silane and ammonia directly after the gallium nitride deposition.

The etching of the dielectric is in particular carried out by photolithography.

Discrete apertures, or apertures in the form of stripes, are defined in the silicon nitride layer, thus exposing the gallium nitride surface on a micrometric feature. The apertures are preferably regular polygons, especially ones of hexagonal shape. Advantageously, the discrete apertures are inscribed in a circle of radius of less than 10 micrometers, whereas the apertures in the form of stripes have a width of less than 10 micrometers, the length of the stripes being limited only by the size of the substrate.

Spacing of the apertures is regular and must allow localized gallium nitride epitaxy followed by anisotropic and lateral growth.

In general, the portion of exposed area of substrate or of gallium nitride to the total area of the substrate is between 5 and 80%, preferably between 5 and 50%.

It has been found that gallium atoms are not deposited on the dielectric and that, in other words, this etched dielectric surface allowed the gallium atoms to concentrate on the apertures.

Next, regrowth on the substrate is carried out using OMVPE. Regular features or islands develop. Examination in a high-resolution electron microscope shows that the GaN dislocation density in the regular features or islands, which has therefore grown without heteroepitaxial strains, is very much less, in the case of the third variant, than that existing in the first GaN layer. Thus, the GaN growth, which takes place laterally in the $[10\bar{1}0]$ directions on a dielectric surface, and therefore without being in epitaxial relationship with the sapphire substrate, results in much better GaN crystal quality than the usual processes. After obtaining an array of regular features, the growth may be continued, either by OMVPE or by HVPE. It is carried out laterally, until coalescence of the islands. These surfaces resulting from the coalescence of islands exhibit superior crystal quality to the layers grown heteroepitaxially on sapphire.

The novelty of the process therefore consists in using the growth anisotropy to induce lateral growth, going as far as coalescence, and thus in obtaining a continuous strain-free GaN layer. The lateral growth takes place from gallium nitride features or islands having reduced defect densities, said features being obtained by localized epitaxy.

According to a variant, the epitaxial regrowth is carried out using undoped gallium nitride.

According to another variant, the epitaxial regrowth is carried out using gallium nitride doped with a dopant chosen from the group consisting of magnesium, zinc, cadmium, beryllium, calcium and carbon, especially with magnesium. This is because it has been found that the doping of gallium nitride with a doping agent, especially magnesium, modified the GaN growth mode and resulted in a relative increase in the growth rate in the $<10\bar{1}1>$ directions with respect to the growth rate in the [0001] direction. Preferably, the dopant/Ga molar ratio is greater than 0 and less than or equal to 1, advantageously less than 0.2.

According to another advantageous variant, the epitaxial regrowth is carried out in two steps.

Firstly, undoped gallium nitride is deposited on the etched dielectric or with a thickness of the order of one angstrom, under vertical growth anisotropy conditions, and then gallium nitride continues to be deposited in the presence of a dopant in order to favor the lateral growth resulting in coalescence of the features.

The invention also relates to the epitaxially grown gallium nitride layers, characterized in that they can be obtained by the above process. Advantageously, these layers have a

defect density of less than those obtained in the prior art, especially less than approximately 10^9 cm^{-2}.

Preferably, the epitaxial layer has a thickness of between 1 and 1000 micrometers and optionally in that it is self-supported after the substrate has been separated.

The invention finds particularly advantageous application in the production of diode lasers provided with an epitaxial gallium nitride layer described above.

BRIEF DESCRIPTION OF DRAWING

Several embodiments of the process according to the invention will now be described in relation with FIGS. **1** and **8** and the examples.

FIG. **1** is a schematic cross-sectional view of a gallium nitride layer according to the invention.

FIG. **2** is a photograph showing regular pyramidal features formed during the localized epitaxy using undoped gallium nitride, when the apertures in the dielectric are discrete apertures.

FIG. **3** is a sectional view perpendicular to the [11$\bar{2}$0] direction of a localized gallium nitride truncated hexagonal pyramid.

FIG. **4** shows the variation in W_T, W_B and H values in μm as a function of the growth time in min. W_T, W_B and H are defined in FIG. **3**.

FIG. **5** shows the variation in the growth rates normalized to the molar flux of TMGA in the [0001] and <10$\bar{1}$1> directions as a function of the Mg/Ga molar ratio in the vapor phase.

FIG. **6** is a photograph of the observed pyramids obtained by localized epitaxial regrowth with magnesium-doped GaN. FIG. **6** shows the advantageous effect of the magnesium dopant on the GaN growth mode in that it allows coalescence of the features to be obtained much more rapidly, resulting in the formation of a strain-free continuous gallium nitride layer in epitaxial relationship.

FIG. **7** is a photograph of the pyramids obtained during growth according to the Example 5, in transmission electron microscopy.

FIG. **8** is a photograph of the pyramids obtained during growth according to Example 5, in scanning electron microscopy.

DETAILED DESCRIPTION OF INVENTION

EXAMPLE 1

Deposition of an Undoped Gallium Nitride Layer

A suitable vertical reactor operating at atmospheric pressure is used for the OrGaNometallic Vapor Phase Epitaxy. A thin gallium nitride layer **2** having a thickness of 2 μm is deposited, by orGaNometallic vapor phase epitaxy at 1080° C. on a (0001) sapphire substrate **1** having a thickness of 200 μm. The gallium source is trimethylgallium (TMGa) and the nitrogen source is ammonia. Such a method is described in many documents.

The experimental conditions are as follows:

The gaseous vehicle is a mixture of H_2 and N_2 in equal proportions (4 sl/min.). The ammonia is introduced via a separate line (2 sl/min.).

After the first gallium nitride epilayer has been grown, a thin layer of a silicon nitride film **3** is deposited as a mask for the subsequent selective growth of gallium nitride using SiH_4 and NH_3 at a rate of 50 sccm and 2 slm, respectively.

The electron transmission microscope observations on cross sections show that the mask obtained forms an amorphous continuous layer having a thickness of approximately 2 nm. Since the stoichiometry of this film was not measured, the term SiN will be used for the rest of this specification. Nevertheless, it seems that the stoichiometry corresponds to the Si_3N_4 term. Although extremely thin, this SiN layer proved to be a perfectly selective mask. The etching is then carried out, by photolithography and reactive ion etching, in order to expose hexagonal apertures **4** circumscribed by a 10 μm diameter circle. The distance between the centers of two adjacent apertures in the mask is 15 μm. The epitaxial regrowth on the exposed gallium nitride regions **5** in order to deposit gallium nitride is carried out on the specimens etched under conditions similar to those used for the standard gallium nitride growth, apart from the TMGa flow rate. This is fixed at a lower value (typically 16 μmol/min. for the experiments with undoped gallium nitride) so as to avoid high growth rates resulting from the very effective collection near the regions **5** of the gallium atoms encountering the surface of the mask. The localized epitaxy reveals a growth rate Vc of gallium nitride **6** in the [0001] direction virtually proportional to the space in between two apertures.

In addition, no nucleation on SiN is observed, even for large spacings. From this it may be concluded that the nucleation and the growth of GaN occurs selectively in the apertures **5**. Consequently, the masked areas behave as concentrators, directing the atoms toward the apertures.

The growth rates are measured either in situ by laser reflectometry, or thereafter by scanning electron microscopy (SEM) on drop views or sections.

FIG. **2** is an SEM photograph showing the development of the pyramids.

FIG. **3** is a sectional view perpendicular to the [11$\bar{2}$0] direction of a localized, truncated hexagonal gallium nitride pyramid. W_T, W_B and H depend on the time t. θ_R is the angle between (0001) and (1011) defining the planes. W_{B0} is the width of the apertures in the SiN mask.

FIG. **4** shows the variation in the W_T, W_B and H values in μm as a function of the growth time in min. Using linear regressions through the experimental points, the following results are obtained:

V_R=2.1 μm/h (lateral rate in the [10$\bar{1}$1] direction);

V_C=13 μm/h (rate in the [0001] direction);

W_{B0}=7.6 μm;

θ_R=62.1°.

When W_T=0 at t_0 (the pyramid has a peak of zero width), the height H varies at a lower rate, given by the formula $V_R/COS\ (\theta_R)$

It will be noted that V_C is extremely high compared with the rate of 1 μm/h measured for standard epitaxy on a (0001) substrate using the same vapor phase composition. Consequently, the V_R/V_C ratio is only approximately 0.15.

EXAMPLE 2

Deposition in the Gaseous Phase of a Layer of Gallium Nitride To Which Magnesium Has Been Added

The experiment of Example 1 is repeated apart from the fact that 2.8 μmol/min. of $(MeCp)_2Mg$ is introduced in the vapor phase. The conditions used are: growth time 30 min., growth temperature 1080° C., TMGa 16 μmol/min. and N_2, H_2 and NH_3 2 sl/min. for each of them.

FIG. **6** shows that the presence of magnesium increases the V_R/V_C ratio well above the cos (θ_R) threshold and consequently the (0001) upper facet broadens. The selectivity of the growth is not affected by the presence of $(MeCp)_2Mg$, but the growth anisotropy is advantageously modified.

EXAMPLE 3

Influence of the Mg/Ga Molar Ratio

FIG. 5 shows the variation in the growth rates normalized to the TMGA molar flux in the [0001] and [10$\bar{1}$1] directions as a function of the Mg/Ga molar ratio in the vapor phase.

In practice, it was chosen to keep a constant flux of $(MeCp)_2$ Mg and to vary the amount of TMGA. This makes it possible to ensure that the available Mg concentration on the surface of the growth islands is identical for all the specimens.

Because the growth is controlled linearly by the amount of gallium supplied, the growth rates are normalized in order to compare them.

V^N_C rapidly decreases from 0.8 to 0.1 μm/h/μmol, while V^N_R increases from 0.16 to 0.4 μm/h/μmol when the Mg/Ga molar ratio varies from 0 to 0.17. The dotted line is the curve of the V_R/V_C ratio obtained by extrapolation. The y-axis on the right is V_R/V_C .

This curve shows that the incorporation of Mg allows the pyramidal structure to be easily controlled by modifying the growth anisotropy. This suggests that Mg acts as a surfactant, favoring the adsorption of gallium on the {1011} faces but, conversely, preventing it on the (0001) faces.

EXAMPLE 4

Two-step Deposition of a Gallium Nitride Layer

Firstly, the process according to the invention is carried out using epitaxial regrowth under operating conditions comparable to those of Example 1.

An SiN mask is deposited on a GaN layer deposited beforehand in an epitaxial manner in a suitable reactor on a crystallization substrate such as sapphire. Linear apertures 5 μm in width and spaced apart by 5 μm are then made in the mask in order to expose the regions of the subjacent layer. The linear apertures are advantageously oriented in the GaN [10$\bar{1}$0] direction, although the variant of the process described in this example can be optionally carried out for other orientations of the linear apertures, especially in the GaN [11$\bar{2}$0] direction.

The epitaxial regrowth is carried out on the exposed regions with unintentionally doped GaN under operating conditions such that the growth rate in the [0001] direction of the GaN features sufficiently exceeds the growth rate in the direction normal to the inclined flanks of said features. Under such conditions, the anisotropy of the growth results in the disappearance of the (0001) facet. The first implementation step of the process is completed when the (0001) facet of the GaN feature has disappeared. At the end of the first step, the GaN features are in the form of a stripe, the cross section of which is triangular. However, it is possible to continue the first step until coalescence of the GaN features, in order to completely recover the mask. In this case, the cross section of the coalesced GaN features is a zigzag line.

The second step consists of the epitaxial regrowth with doped GaN, especially with magnesium-doped GaN according to Example 2 or 3, on the GaN features created in the first step. Due to the effect of introducing the dopant, the growth anisotropy is conducive to planarization of the GaN features. The facet C reappears at the top of each of the GaN features obtained in the first step. During this second step, the doped GaN features develop with an expansion of the facet C and, on the contrary, a reduction in the area of the flanks. The second step of the process according to the example is completed when the flanks have disappeared, the upper surface of the deposit formed by the coalesced doped-GaN features then being plane.

The implementation of the two-step process according to the invention as described above results, on the one hand, in the formation of a plane GaN layer, which can therefore serve as GaN substrate for the subsequent deposition, by epitaxial regrowth, of a device structure, especially a diode laser structure, but results, on the other hand, in a highly advantageous improvement in the crystal quality of said substrate. This is because the lines of crystal defects in the subjacent GaN layer propagate via the aperture made in the mask, vertically into the undoped GaN feature created in the first step. However, it seems that these lines of defects become curved during the second step devoted to the deposition of a doped-GaN features. This results in lines of defects which propagate in directions parallel to the surface of the masked GaN layer.

Because of the modification of the direction of propagation of the defects, the upper surface formed by the coalescence of the GaN features is virtually free of emerging defects in regions compatible with the size of electronic devices, such as GaN diode lasers.

EXAMPLE 5

Deposition of a Gallium Nitrite Layer Directly on a Substrate Masked by a Dielectric

This example illustrates a method making it possible to obtain spontaneous formation of gallium nitride features or islands on a substrate by a treatment consisting in covering the substrate with a dielectric, especially silicon nitride, film whose thickness is of the order of 1 Angström. Advantageously, this method makes it possible to avoid having to use ex situ etching of the mask by expensive techniques such as photolithography and chemical etching.

A suitable epitaxial growth reactor is used for the orGaNometallic vapor phase epitaxy. Explicitly, a substrate, especially (0001) sapphire chemically prepared beforehand by degreasing and pickling in an H_2SO_4:H_3PO_4 acid solution, in a 3:1 ratio, is heated to a temperature of approximately 1050–1080° C. in order to be nitrided by exposure to a stream of NH_3 for approximately 10 minutes. After this nitriding step, a very thin film of silicon nitride is formed on the surface of the substrate, the film being obtained by reaction between NH_3 and silane SiH_4 at a temperature of 1080° C. for a time short enough to limit the thickness of the film to that of one atomic plane.

The operating conditions are the following:

The gaseous vehicle is a mixture of nitrogen and hydrogen in equal proportions (4 sl/Min.). The ammonia is introduced with a flow rate of 2 sl/min. while the silane, in a form diluted to 50 ppm in hydrogen, is introduced with a flow rate of 50 scc/min. Under these conditions, the typical NH_3 and SiH_4 reaction time is of the order of 30 seconds.

The successive steps are monitored by laser reflectometry (LR) and transmission electron microscopy (TEM).

After the dielectric layer has been completely formed, a continuous gallium nitrite layer having a thickness of 20 to 30 nm is deposited on the dielectric film. The deposition of the GaN layer is made at a low temperature, of the order of 600° C.

After the deposition of the GaN layer has been completed, it is annealed at a high temperature of the order of 1080° C. Under the combined effect of the temperature rise, of the presence in the gaseous vehicle of a sufficient amount of hydrogen and of the presence of the very thin dielectric film beneath the GaN layer, the morphology of said GaN layer undergoes deep modification resulting from solid-phase recrystallization by mass transport. When the temperature approaches 1060° C., it should be noted that the reflectivity of the buffer layer suddenly decreases. The initially continuous buffer layer is then converted into a discontinuous layer formed from gallium nitride islands.

At the end of this spontaneous in situ recrystallization process, GaN features or islands of very good crystal quality are obtained, these retaining an epitaxial relationship with the substrate by virtue of the very small thickness of the dielectric layer. The GaN features or islands are isolated from one another-by regions or the dielectric layer is bared. The characteristic heights of the islands are of the order of 2400 angstroms. The observation obtained with a transmission electron microscope shows that the islands tend to take the shape of truncated pyramids (FIG. 7).

FIG. 8 is a scanning electron microscope image of a specimen obtained under operating conditions that are modified so as to increase the dimensions of the islands to micrometric values comparable to those of the islands or features obtained in the apertures of a mask (cf. Example 1) produced ex situ by photolithography.

During the subsequent epitaxial regrowth with gallium nitride on the surface of a specimen, those regions of the dielectric where the layer of the dielectric is bared will function as the mask of FIG. 1 and the GaN features or islands thus spontaneously formed are the analogues of the GaN features (cf. FIG. 1 or FIG. 2) located in the apertures (cf. FIG. 1) which are produced ex situ in the mask (cf. FIG. 1). Explicitly, the GaN features or islands will develop by lateral and vertical growth.

GaN layers have thus been obtained by coalescence of the GaN features having a defect density of the order of 10^8 cm^{-2}, i.e. two orders of magnitude less than that of the defects present in the gallium nitride layers produced using the conventional methods.

Thus, in the variants of the process that have been described in the above examples, especially Example 4 describing a two-step variant, the use of the ex situ process of etching the apertures in a mask may advantageously be avoided and replaced with the in situ spontaneous formation, described above, of the GaN islands or features, the control of their geometry and dispersion not being a prerequisite for improving the quality of the GaN layers formed by this process.

What is claimed is:

1. Process for producing an epitaxial layer of gallium nitride (GaN) comprising:

depositing on a substrate, a dielectric layer functioning as a mask; and

regrowing gallium nitride doped with a doping agent as an enhancer of lateral growth with respect to vertical growth on the masked substrate under vapor phase epitaxial deposition conditions so as to induce the deposition of gallium nitride features and an anisotropic and lateral growth of said features, the lateral growth being continued until coalescence of the various features.

2. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1 wherein the substrate is chosen from the group consisting of sapphire, ZnO, 6H—SiC and $LiAlO_2$.

3. Process for producing an epitaxial layer of galium nitride (GaN) according to claim 1, wherein the dielectric layer is a layer of the Si_xN_y type.

4. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, wherein the dielectric layer is an atomic monolayer or a cover of the order of one atomic plane.

5. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, further comprising:

after depositing the dielectric the dielectric layer, etching the dielectric layer to define apertures and to expose the facing regions of the substrate, and

wherein gallium nitride is regrown under epitaxial deposition conditions on the masked and etched substrate so as to induce the deposition of gallium nitride features on the facing regions and the anisotropic and lateral growth of said features (6), the lateral growth being continued until coalescence of the various features.

6. Process of producing an epitaxial layer of gallium nitride (GaN) according to claim 1, comprising:

depositing the dielectric layer (3) on a thin gallium nitride layer;

etching the dielectric layer to define apertures (4) and to expose those regions (5) of said thin gallium nitride layer which face them; and

regrowing gallium nitride under epitaxial deposition conditions on the epitaxially grown, masked and etched substrate so as to induce the deposition of gallium nitride features on the facing regions and the anisotropic and lateral growth of said regions (6), the lateral growth being continued until coalescence of the various features.

7. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 5, wherein the apertures are one of discrete apertures and apertures in the form of stripes.

8. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 7, wherein the discrete apertures are regular polygons.

9. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 7, wherein the discrete apertures are inscribed in a circle of radius of less than 10 μm.

10. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 7, wherein the apertures in the form of stripes have a width of less than 10 μm.

11. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 6, wherein the apertures are one of discrete apertures and apertures in the form of stripes.

12. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 11, wherein the discrete apertures are regular polygons.

13. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 12, wherein the discrete apertures are inscribed in a circle of radius of less than 10 μm.

14. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 11, wherein the apertures in the form of stripes have a width of less than 10 μm.

15. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, further comprising, after depositing the dielectric layer, exposing a portion of the substrate, wherein the exposed portion of substrate or of gallium nitride with respect to the total area of the substrate is between 5 and 80 percent.

16. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, wherein the exposed portion of substrate or of gallium nitride with respect to the total area of the substrate is between 5 and 50 percent.

17. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, wherein the doping agent comprises magnesium and the magnesium-doped gallium nitride is regrown on the masked, epitaxially grown, and etched substrate.

18. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 11, wherein a dopant/gallium molar ratio in the vapor phase is greater than 0 and less than or equal to 1.

19. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim 1, wherein the doping

agent comprises magnesium and the magnesium-doped gallium nitride is regrown on the masked, and etched substrate.

20. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim **19**, wherein a dopant/gallium molar ratio in the vapor phase is greater than 0 and less than or equal to 1.

21. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim **1**, wherein the regrowing gallium nitride comprises depositing under vapor phase epitaxial conditions and the vapor phase epitaxial deposition conditions involve the use of a carrier gas comprising a hydrogen gas.

22. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim **21**, wherein the vapor phase epitaxial deposition conditions involve the use of a carrier gas further comprising a nitrogen gas.

23. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim **1**, wherein prior to regrowing gallium nitride doped with a doping agent, the masked, and etched substrate undergoes regrowth, regrowing undoped gallium nitride.

24. Process for producing an epitaxial layer of gallium nitride (GaN) according to claim **23**, wherein prior to regrowing gallium nitride doped with a doping agent, the masked, epitaxially grown and etched substrate undergoes regrowth, regrowing undoped gallium nitride.

25. Epitaxial doped gallium nitride layer, wherein obtained by the process according to claim **1**.

26. Optoelectronic component, wherein they are provided with an epitaxial layer of gallium nitride according to claim **25**.

27. Optoelectronic component of claim **26**, comprising a diode laser.

28. Epitaxial gallium nitride layer according to claim **25**, wherein it has a thickness of between 1 μm and 1000 μm and in that it is separable from its substrate.

29. Optoelectronic component, wherein they are provided with an epitaxial layer of gallium nitride according to claim **28**.

30. Optoelectronic component of claim **29**, comprising a diode laser.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,325,850 B1
DATED : December 4, 2001
INVENTOR(S) : Beaumont et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [73], Assignee, delete "**Recherché**" and insert -- **Recherche** --.

Column 9,
Line 65, after "the dielectric" delete the second occurrence of "the dielectric".

Column 10,
Line 63, delete "claim 11" and insert -- claim 17 --.

Signed and Sealed this

Tenth Day of September, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

US005880485A

United States Patent [19]

Marx et al.

[11] Patent Number: 5,880,485

[45] Date of Patent: Mar. 9, 1999

[54] **SEMICONDUCTOR DEVICE INCLUDING GALLIUM NITRIDE LAYER**

[75] Inventors: **Diethard Marx**, Osaka; **Zempei Kawazu**; **Yutaka Mihashi**, both of Tokyo, all of Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

[21] Appl. No.: **927,692**

[22] Filed: **Sep. 11, 1997**

[30] **Foreign Application Priority Data**

Mar. 24, 1997 [JP] Japan 9-069703

[51] **Int. Cl.**^{6} **H01L 33/00**

[52] **U.S. Cl.** **257/94**; 257/76; 257/201; 257/615; 372/45

[58] **Field of Search** ..... 257/22, 76, 94, 257/200, 201, 615; 252/623 GA; 372/45

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Primary Examiner—Sara Crane
Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

A high-quality gallium nitride layer is grown on a surface of a substrate which is exposed through a dielectric mask on the substrate. The high-quality gallium nitride layer has a composition expressed by the chemical formula:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$. An aluminum nitride thin layer is interposed between neighboring pairs of gallium nitride selectively grown layers and has a composition expressed by the following chemical formula:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq1$.

8 Claims, 9 Drawing Sheets

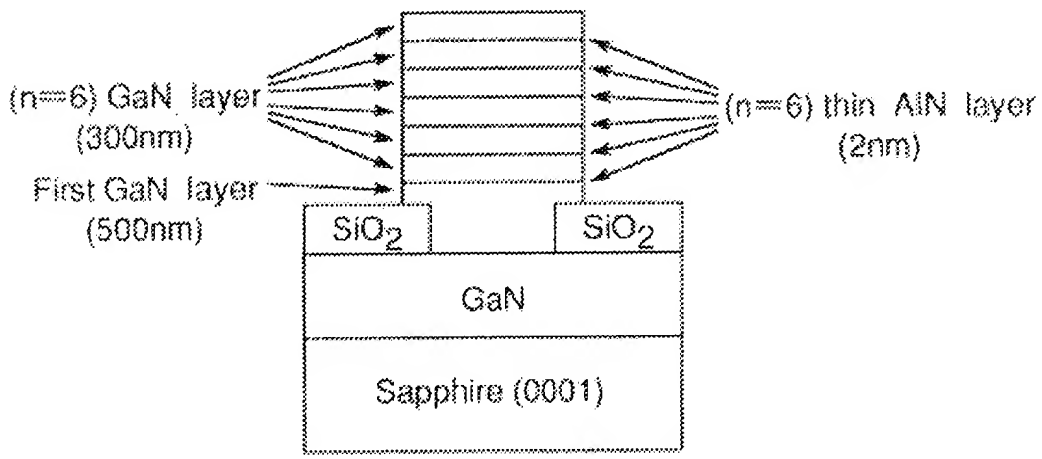


Fig.1

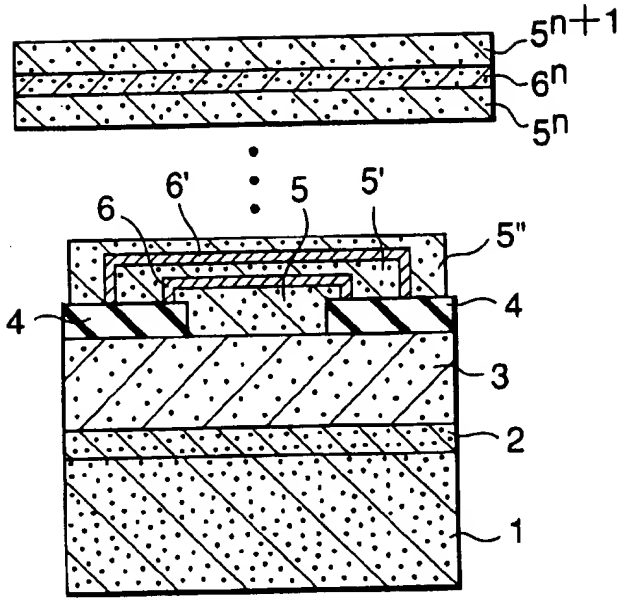


Fig.2A

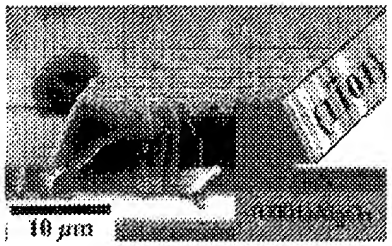


Fig.2B

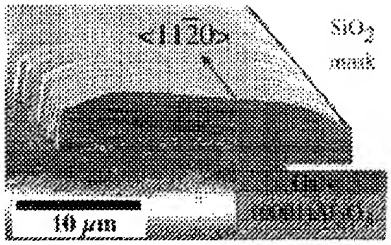


Fig.2C

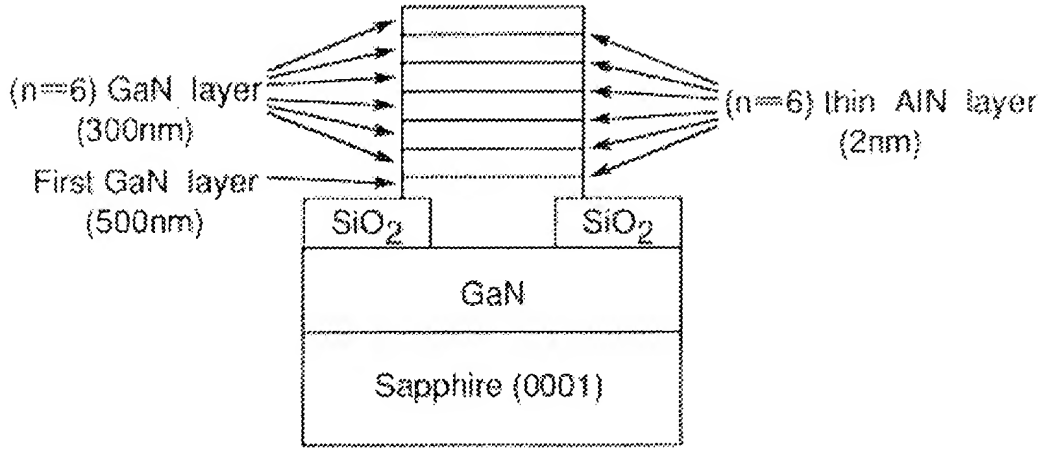
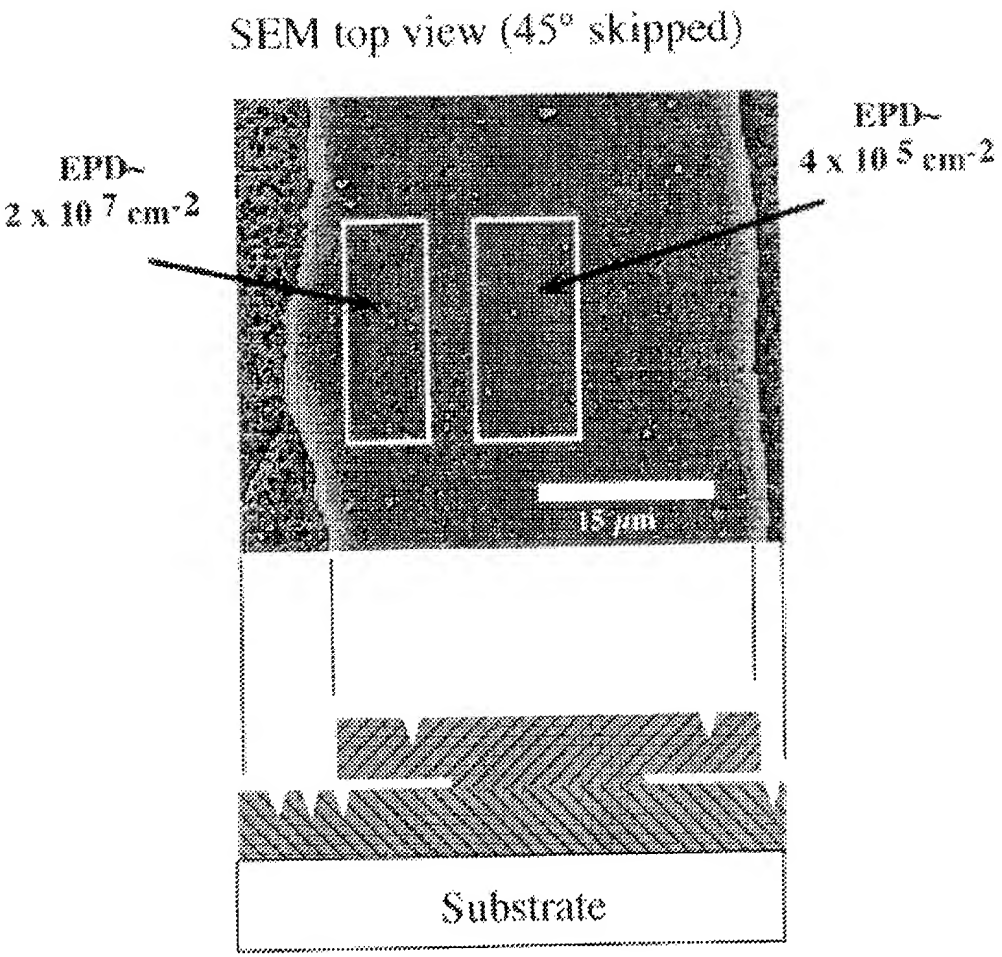


Fig. 3



Cross sectional schematic view after etching in molten KOH: SiO_2 film removed by etching.

Fig. 4

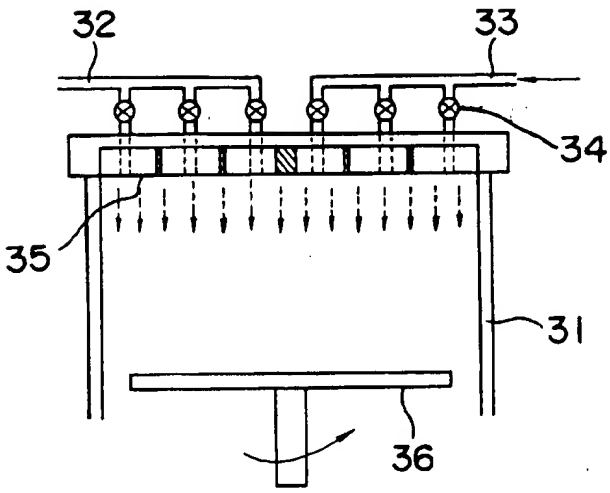


Fig. 5

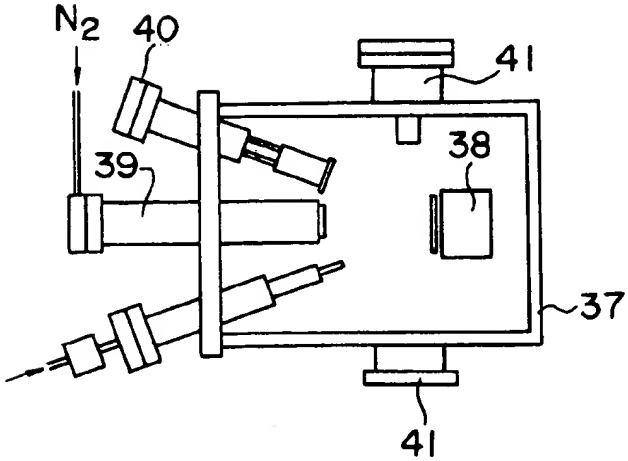


Fig.6

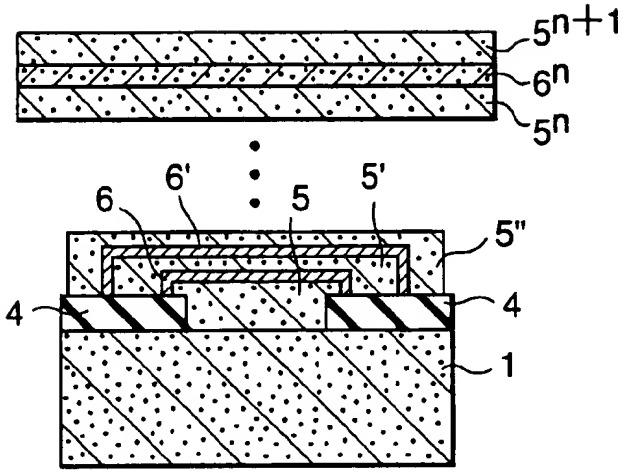


Fig.7

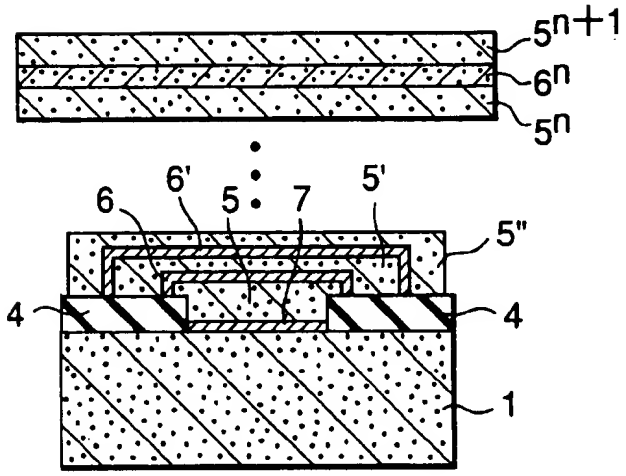


Fig. 8A Layer structure

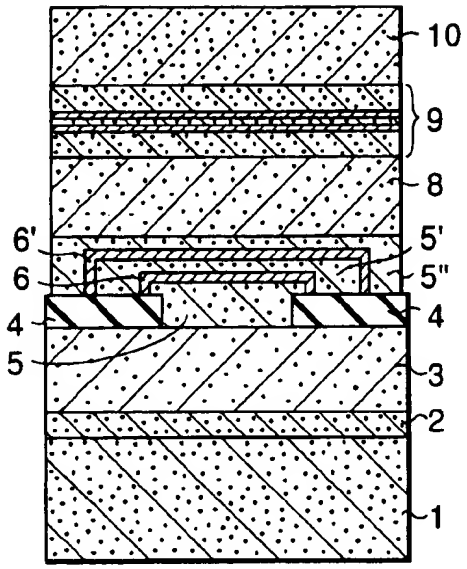


Fig. 8B Laser Ridge definition by Lithography and Dry Etching Process

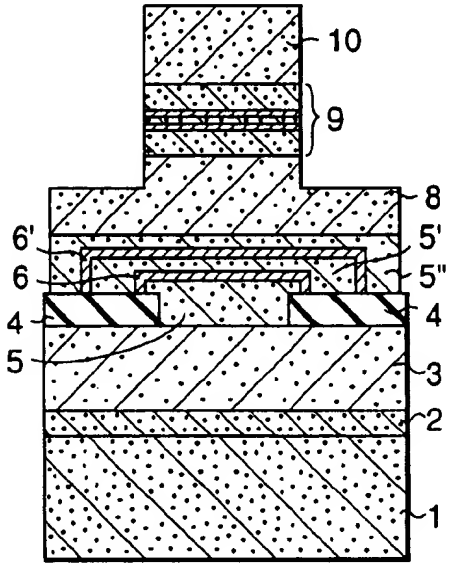


Fig. 8C Index Guiding Laser by Lithography

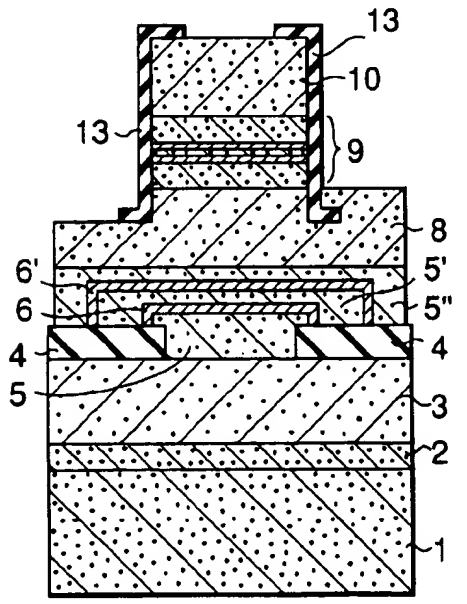


Fig. 8D Metal contact definition by Lithography

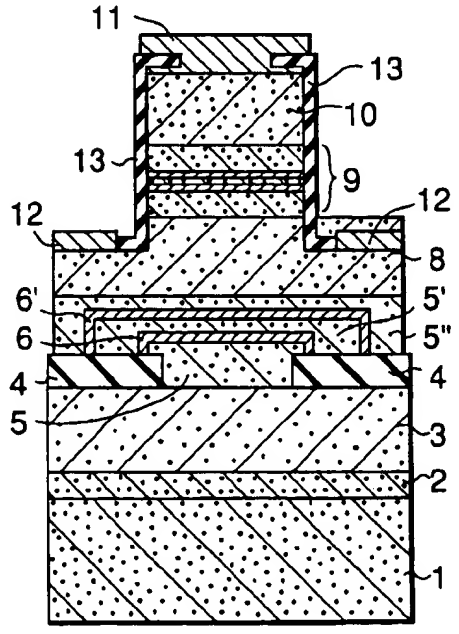


Fig. 9

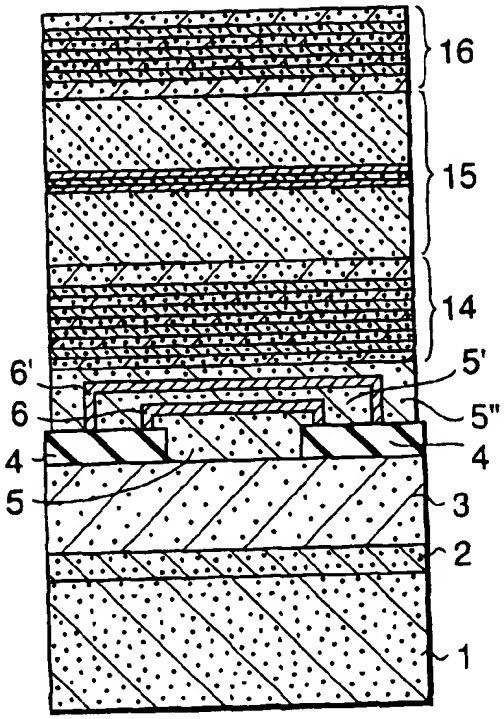


Fig. 10

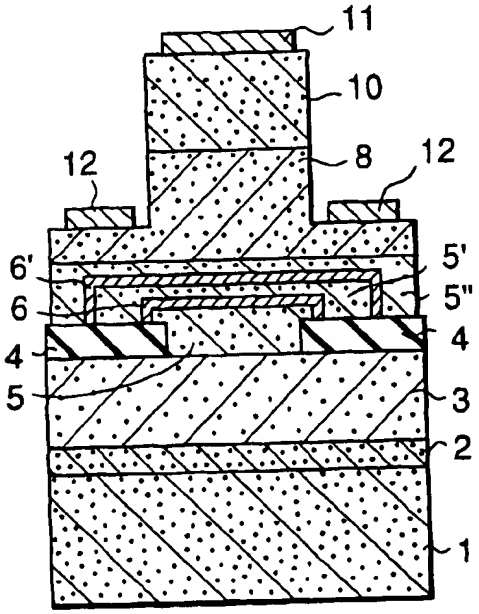


Fig.11

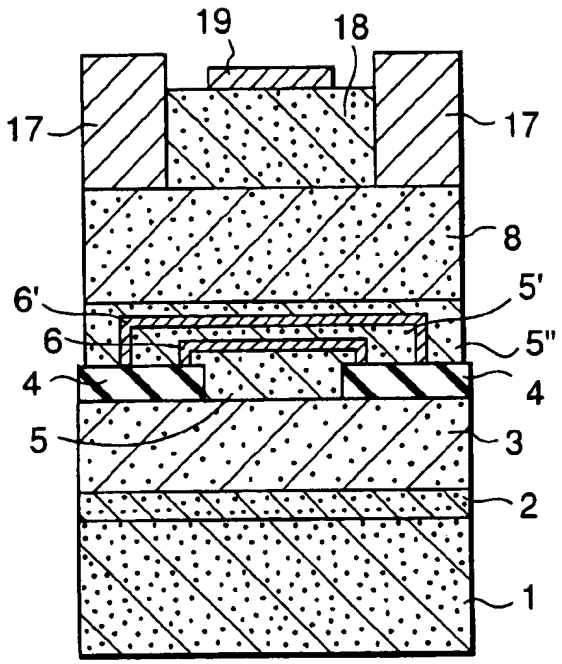


Fig.12A

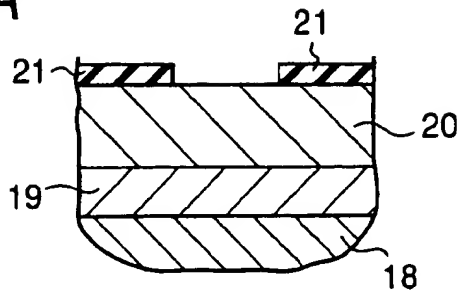


Fig.12B

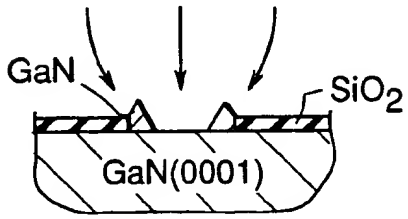


Fig.12C

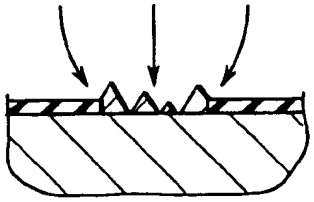


Fig.12D

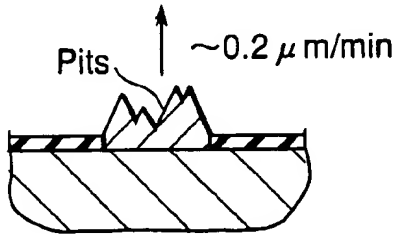


Fig.12E

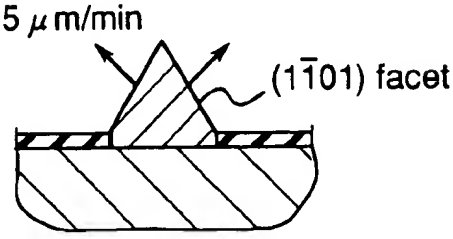
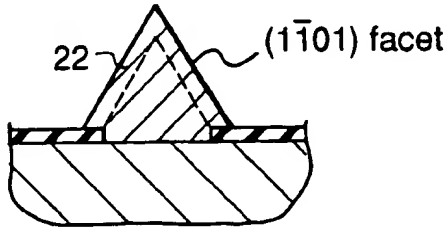


Fig.12F



SEMICONDUCTOR DEVICE INCLUDING GALLIUM NITRIDE LAYER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a high-quality gallium nitride layer-structure provided with a flat surface and a very low dislocation density selectively grown on a semiconductor substrate and a method of selectively growing the layer on the substrate.

2. Description of the Prior Art

Only few data are available on the selective growth of GaN. Therefore, there have been required information on, how the crystalline quality of GaN can be improved drastically using selective growth and a suitable layer structure.

The first study to our best knowledge was given by Y. Kato et al. (J. Crystal Growth 144 (1994) 133). They used GaN layers for patterning with a SiO_2 mask as shown in FIG. **12**A. The substrate **18** was sapphire (11$\bar{2}$0), **18**, followed by a buffer layer of AIN **19**, and a 2 μm thick GaN crystal layer **20**. Then a 100 nm thick SiO_2 layer **21** was sputtered and stripes opened by a lithography and etching process. FIGS. **12**B to **12**F show processes of the successive growth of GaN on the mask in a cross sectional view. As can be seen, first a rough surface occurs in FIG. **12**B, which finally closes to the triangular form **22** given in FIG. **12**F,. In all cases, the selectively grown GaN did not grow in a layer by layer mode, and thus the growth mode is not suitable for the growth of device structures.

A more recent result on GaN selective growth was given by T. Tanaka et al (TWN 1995 conference, Nagoya, Sep. 21, 1995). They tried to deposit GaN directly on sapphire substrates. Depending on the surface treatment condition (nitridization in ammonia or not) and growth temperature, they could obtain two different stripe forms. One is of the triangular shape and the other is a rectangular form. In both cases, no data hint to an improved crystal quality, and the quality is expected to be poor due to the missing GaN buffer layer. Furthermore the result shows that the shape strongly depends on substrate treatment, which can cause a problem of reproducibility.

Finally, our own study of selective growth of GaN showed similar problems as in Y. Kato et al. For the experiments, first 2 μm of GaN (including a low temperature GaN layer) was deposited on sapphire, and then a 100 nm SiO_2 film was sputtered on the GaN surface. The SiO_2 film was partly removed by lithography and wet etching steps. The open areas formed stripes oriented in the (11$\bar{2}$0) direction. After this procedure, the samples were again loaded into the MOCVD apparatus machine. After heating the sample in an ammonia flow to 1130° C. selective growth was initiated by introducing a flow of trimethyl gallium (TMG). In a cross sectional SEM picture, the obtained GaN stripe has a very rough surface morphology.

Therefore, a first object of the present invention is to provide a new method and layer structure which improves GaN crystal line quality drastically.

The method can be applied to many device structures. Therefore, a second object of the present invention is to provide a device formed on the improved gallium nitride, such a laser, UV-detector FET, HFET, HBT, HEMT and so on.

SUMMARY OF THE INVENTION

According to the first aspect of the present invention, there can be provided a method of selectively growing a high-quality gallium nitride layer on a surface area of a substrate which is exposed through a dielectric mask formed on the substrate, the high-quality gallium nitride layer having a composition expressed by the following chemical formula:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$, the method comprising a step of alternately growing the gallium nitride selectively grown layer and an aluminum nitride thin layer on the substrate, the aluminum nitride thin layer having a composition expressed by the chemical formula:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq 1$.

According to the present invention, with the selective growing method to form the gallium nitride layer of the present invention, the aluminum nitride thin layer, effective to increase the length of migration of the Ga atoms as compared with that of the gallium nitride layer, is suitably interposed between each neighboring gallium nitride layer which is selectively grown to thereby accomplish a flattening of the gallium nitride layer immediately above the aluminum nitride thin layer. Accordingly, not only can the surface irregularities present at the surface of the substrate laminated with the gallium nitride layer be reduced, but also it is possible to obtain the substrate laminated with a gallium nitride layer excellent in surface flatness.

In an embodiment of the present invention, the method may comprise a step of growing a gallium nitride layer on a buffer layer prior to the formation of the dielectric mask on the substrate sp a smoother surface can be obtained.

In the embodiment of the present invention, an aluminum nitride layer may be grown on the substrate or an the gallium nitride layer on the substrate.

In the embodiments, the selectively grown gallium nitride layer has a film thickness within a preferred range of 2 to 1,000 nm. On the other hand, the aluminum nitride thin layer has a film thickness within the preferred range of 1 to 200 nm. Because the inclusion of the 1–200 nm thick AIN layers is effective to dramatically change the mode of growth and also to increase the flatness of a surface of each GaN layer as will be discussed in detail later, the density of defects in the GaN layers is substantially reduced as compared with the prior art growing method.

The substrate may be selected from the group consisting of sapphire, Si, GaAs, heat-resistant glass, SiC and GaN, because such a substrate is advantageous in many aspects, for example, inexpensive and easy to handle.

The method can be applied to a gallium nitride selectively grown layer including a GaN layer while the aluminum nitride thin layer is an AIN layer.

According to the second aspect of the present invention, there can be a substrate laminated with a high-quality gallium nitride layer which comprises:

a substrate;

a dielectric mask formed on the substrate and having a portion of a surface exposed to define an opening;

a plurality of gallium nitride selectively grown layers each grown on a portion of the substrate encompassed by the opening, each gallium nitride selectively grown layer having a composition expressed by the following chemical formula:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0<y<1$, $0\leqq z<1$, and $x+y+z=1$; and

an aluminum nitride thin layer interposed between the neighboring gallium nitride selectively grown layers, said aluminum nitride thin layer having a composition expressed by the following chemical formula:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq 1$.

The high-quality gallium nitride layer of the present invention is effective to increase the yield of manufacture of devices to be formed on the substrate laminated with the gallium nitride layer.

In an embodiment of the present invention, a buffer layer and gallium nitride layer formed on the substrate prior to the formation of the dielectric mask, is used as a substrate for the deposition of the high-quality gallium nitride layer. A high quality surface can be obtained.

In the both embodiments, the aluminum nitride thin layer is formed on the substrate or the gallium nitride layer on the substrate.

According to the third aspect of the present invention, there can be a semiconductor device which comprises:

the substrate; and

a photoelectric semiconductor element, an electronic semiconductor element or an electro-optical integrated semiconductor element.

Because of the flatness of the surface and the reduced defect density of the substrate laminated with the gallium nitride layer, it is also possible to increase the characteristic and the reliability of elements formed on the substrate.

In an embodiment of the present invention, a photo electric semiconductor element may comprise:

a laser element region having successively deposited on the laminated substrate a stripe-shaped n-type gallium nitride clad layer, a stripe-shaped gallium nitride active layer and a p-type gallium nitride clad layer. It is possible to improve the device characteristic, to increase the lifetime and to lower the threshold current density and the power consumption.

In an another embodiment of the present invention, the photo electric semiconductor element may comprise:

a lower Bragg reflection layer structure formed on the laminated substrate;

a n-type gallium nitride clad layer, gallium nitride active layer and p-type gallium nitride clad layer deposited successively on the lower Bragg reflection layer structure;

a laser element region including an upper Bragg reflection layer structure formed over the p-type gallium nitride clad layer. Because the Bragg reflection layer structure is formed over the high-quality gallium nitride crystal, any possible deterioration of the laser characteristic due to the poor crystalline quality can be considerably suppressed.

The laminated structure may include the gallium nitride layer and the aluminum nitride thin layer on the laminated substrate, which concurrently serve as the lower Bragg reflection layer structure.

In another embodiment of the present invention, the photo electric semiconductor element may comprise:

a detector element region having successively deposited on the laminated substrate a n-type gallium nitride clad layer and a p-type gallium nitride clad layer, because it is possible to increase the sensitivity and also to improve the device characteristics such as increase of the operating frequency to a high band region due to a reduction in traps.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become readily understood from the following description of preferred embodiments made with reference to the accompanying drawings, in which like parts are designated by like reference numeral and in which:

FIG. **1** is a sectional view showing a high-quality GaN substrate according to the first embodiment of the present invention.

FIG. **2A** is a sectional SEM picture of a GaN selectively grown layer according to the first embodiment of the present invention.

FIG. **2B** is a sectional SEM picture of a conventional GaN layer.

FIG. **2C** is a schematic sectional view of a GaN selectively grown layer according to the first embodiment of the present invention.

FIG. **3** is a SEM picture of EPD in a GaN layer according to the first embodiment of the present invention.

FIG. **4** is an MOCVD reactor according to the first embodiment of the present invention.

FIG. **5** is an MBE chamber according to the first embodiment of the present invention.

FIG. **6** is a sectional view showing a GaN substrate according to the third embodiment of the present invention.

FIG. **7** is a sectional view showing a GaN substrate according to the third embodiment of the present invention.

FIG. **8** is an sectional view of ridge-type laser diode according to the fourth embodiment of the present invention.

FIG. **9** is a sectional view of VSCEL according to the fifth embodiment of the present invention.

FIG. **10** is a sectional view of a UV-detector according to the sixth embodiment of the present invention.

FIG. **11** is a sectional view of HFET according to the sixth and seventh embodiment of the present invention.

FIG. **12** shows each step of conventional GaN selective growth.

DETAILED DESCRIPTION OF THE EMBODIMENTS

(First Embodiment)

Referring now to FIG. **1** which illustrates, in a sectional representation, a GaN selectively grown layer in which a layer structure including a plurality of GaN layers **5**, **5'**, . . . , and 5^{n+1} and a plurality of thin AlN layers **6**, **6'**, . . . , and 6^n each intervening between the neighboring GaN layers are selectively grown on a substrate **1** partly covered by a dielectric, such as SiO_2 film **4**. The substrate **1** is a sapphire (0001) substrate on which a low temperature buffer (LTB) layer **2** and a GaN layer **3** are deposited, one on the other, and including a dielectric mask made of, for example, SiO_2 film **4** for selective growth and also a GaN layer grown in an opening.

The thin AlN layer is formed between each neighboring pair of GaN layers at predetermined intervals. The inclusion of the AlN layers is effective to dramatically change the mode of growth and also to increase the flatness of a surface of each GaN layer as will be discussed in detail later, thereby considerably reducing the density of defects in the GaN layers as compared with the prior art growing method.

The surface condition of each GaN layer formed by the use of the prior art selective growing method and the surface condition of each GaN layer formed by the use of the selective growing method according to the embodiment of the present invention are shown in FIGS. 2A and 2B, respectively, for comparison purpose. The substrate employed was a sapphire (0001) substrate on which, after the GaN layer had been formed, a SiO_2 mask was formed for selective growth of the GaN layer (or the AIN layer).

FIG. 2A is a scanning electron microscope (SEM) photo of the conventional GaN layers having no AIN layer intervening between the neighboring GaN layers and FIG. 2B is a SEM photo showing the structure in which, after the thin GaN layer of 500 nm had been formed, the thin AIN layers of 2 nm and the GaN layer of 300 nm are alternately formed over the 500 nm GaN layer. FIG. 2C is a schematic diagram depicting the GaN layers shown in FIG. 2B. While the growth thickness on the substrate is nominal, the reality is that because of influences brought about by migration, the film thickness tends to differ from the nominal thickness as the growth proceeds.

As FIGS. 2A and 2B make it clear, each GaN layer formed by the prior art selective growing method shown in FIG. 2A has resulted in a rough morphology on the surface, whereas the surface of the GaN layers including the thin AIN layers formed according to the selective growing method of the present invention has exhibited a favorable flatness. The reason therefor appears that the length of migration of Ga on the surface of the AIN layer is so large that the formation of the AIN layers at the predetermined intervals during the growth of the GaN layers results in flattening of the GaN layer. Also, the increase of the migration length also results in an increase of the growth of the GaN layer overlaying the SiO_2 mask. This is clearly illustrated by the fact that the GaN layers so formed spread laterally in FIG. 2B further than that shown in FIG. 2A.

The use of the selective growing method of the present invention makes it possible to improve the crystalline quality of the GaN layers in addition to flattening of the surface. To qualitatively examine the improvement in crystalline quality, a sample shown in FIG. 2B was etched in a molten KOH solution which is a selective etching solution for defects, to determine the EPD (Etch Pit Density).

FIG. 3 is a SEM photo showing a surface condition of the sample of FIG. 2B which has been etched in the manner described above. The EPD was found to be about $4\times10^5cm^{-2}$. In the SEM photo shown in FIG. 3, the surface of the sample was observed from a slant direction and the sample was etched (at 450° C. for 30 seconds) in the molten KOH solution to determine the EPD. The SiO_2 selective growth mask was completely removed by etching to allow the underlying GaN layer to be exposed to the outside.

Thus, since the EPD when formed according to the prior art method is generally about $4\times10^8cm^{-2}$, the use of the selective growing method of the present invention is effective to decrease the EPD by a factor of 1000.

In the illustrated embodiment, the GaN layers are formed by a selective growing method utilizing an MOCVD process. An MOCVD apparatus used therefor is shown in FIG. 4. In the MOCVD apparatus shown in FIG. 4, all gases are supplied from the top. Specifically, nitrogen gas is supplied through a nitrogen source manifold 32 separate from a supply manifold 33 through which a Group III source gas is supplied. The flow of each gas can be optimized by adjusting a respective regulating needle valve 34 and, separate therefrom, a predetermined flow of hydrogen is supplied from a screen 35. The gases so supplied reach a substrate mounted on a wafer carrier 36 and react with the substrate to form a desired semiconductor layer. To increase uniformity of the semiconductor layer, the wafer carrier is rotated at a high speed (for example, 500 to 1,000 rpm). The pressure inside a reactor is preferably within the range of 76 to 200 Torr.

In the practice of the illustrated embodiment of the present invention, high-quality GaN can be obtained by a high temperature growth at 1030° C. on a thin GaN buffer layer. Such a GaN buffer layer is preferably deposited at 540° C. at 200 Torrs pressure, ammonium gas (NH_3), and trimethyl gallium.

It is to be noted that any method associated with any one of the MBE method and the CBE method can be employed in the present invention.

FIG. 5 illustrates an MBE apparatus equipped with an ECR plasma source. In a method in which to MBE apparatus is employed, a substrate is first transferred into a high-vacuum MBE chamber 37 and the substrate 38 is, after having been annealed typically at 900° C. with an N_2 of a gas exposure or a high-temperature thermal annealing technique, exposed to N_2 and is, therefore, nitrided by nitrogen gas supplied through a gas injector 39 while the substrate is typically heated to a temperature of 400° C.

Then, a low-temperature buffer layer of either GaN or AIN is deposited by introduction of a Ga source beam. The Ga source beam referred to above consist of Ga atoms from a MBE furnace 40 or an organic metal Ga precursor such as, for example, triethyl gallium (TEG) or TMG, and they can be introduced by any suitable gas injector.

Thereafter, a high-quality GaN layer is deposited while the substrate temperature is typically within the range of 600° to 860° C.

An advantage of the method of the present invention lies in that by the use of an electron diffraction (RHEED) 41 the crystalline quality can be analyzed in situ during the growth.

The most preferred source of nitrogen is precracked N_2, NH_3 or the like and, on the other hand, the precursor of Ga is often used in the form of TMG or TEG. In addition, nitrogen radicals or atoms can be formed by an ECR plasma, microwave activation of N_2 or thermal cracking off NH_3.

The selective growing method according to the embodiment of the present invention will now be described with particular reference to FIG. 1.

A sapphire substrate 1 having a crystalline orientation (0001) is placed on a susceptor for crystalline growth. The crystalline orientation of the sapphire substrate may be other than (0001).

Then, residual impurities are cleaned from the surface of the substrate. For this surface cleaning method, treatment with hydrogen atoms in the MBE apparatus or a high temperature treatment in the MOCVD apparatus is preferred.

Then, a buffer layer 2 having a thickness within the range of 2 to 500 nm is deposited on the sapphire substrate 1 at a substrate temperature of 200° to 1,000° C. The buffer layer may be a GaN layer or may be a multi-layered compound of a material expressed by the following formula:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$. The purpose of the buffer layer is to form a nucleation layer on the substrate.

Then, a high-temperature GaN layer is grown at a temperature higher than 900° C. in the case of the MOCVD

process or at a temperature higher than 600° C. in the case of the MBE process. The film thickness is typically about 2 μm, but may be within the range of 2 nm to 6 μm. It is to be noted that in place of the GaN layer, any other material expressed by the following formula can be employed:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$.

After having been cooled, the sample is removed from the reactor and a thin dielectric layer **4** is deposited on it. The dielectric material may be SiO_2, SiN_x, SiO_xN_x or any other known dielectric material. The film thickness is typically 100 nm, but may be within the range of 10 to 500 nm.

Thereafter, the dielectric layer is partially removed by the use of a lithographic technique and wet etching to leave an opening. The opening left by removing that portion of the dielectric layer may have a shape chosen in consideration of the structure of a semiconductor device. This opening may be in the form of a stripe shape having a width within the range of 200 nm to 50 μm and a length within a range of 200 nm to several millimeters. The stripe-shaped opening may be oriented in any desired direction and may not be limited to a specific direction.

The sample so prepared is again loaded in the reactor and is heated to a growth temperature at which selective growth of the GaN layer takes place. The selective growth starts with a growth of a thin GaN layer (2 to 1,000 nm) or a thin AlN layer (1 to 200 nm) on the GaN layer **3** which has been masked by a dielectric material such as, for example, SiO_2 film **4**.

After this growth, the GaN layers (2 to 1,000 nm) 5' and so on and the AlN layers (1 to 200 nm) 6' and so on are alternately deposited. The total number of combinations of GaN/AlN may be chosen within the range of 1 to 200.

The GaN layer **5** when grown to a film thickness of about 200 nm will have its surface formed with surface irregularities and, therefore, before the surface irregularities are formed on the surface of the GaN layer **5**, the thin AlN layer **5** has to be formed. Since on the surface of the AlN layer Ga generally migrates considerably, a flat GaN layer is formed on the AlN layer. Accordingly, if before the surface irregularities are formed on the GaN layer the AlN layer is sandwiched, it is possible to form the GaN layer while the surface flatness is maintained. The AlN layer may have a film thickness generally within the range of 1 to 50 nm although the use of at least one AlN layer may be considered sufficient to obtain the effect of the above described migration.

Also, by inserting the AlN layers into the GaN layers at the predetermined intervals, it is possible to enclose screw dislocations, occurring in the GaN layer immediately below the AlN layer, within the GaN layer. In other words, since the AlN layer is formed over the GaN layer, the dislocations occurring within the GaN layer can be looped, rendering it to be difficult for them to propagate over the AlN layer and, consequently, the density of dislocations within the GaN layer formed in the outermost surface can be reduced.

From the foregoing, it has now become clear that the outermost GaN layer 5^{n+1} grown by the use of the growing method of the foregoing embodiment of the present invention has an optimized surface morphology as compared with the surface of the GaN layer grown by the prior art method and also has a crystalline quality in which the density of defects such as screw dislocations is minimized.

It is, however, to be noted that in place of the GaN layers 5, 5', . . . and 5^{n+1}, different GaN-type compound layers expressed by the following formula can be equally employed:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$.

Also, in place of the thin AlN layers 6, 6', . . . and 6^n, AlN-type thin layers prepared from a composition containing a relatively high quantity of Al, which is expressed by the following formula may be employed:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq 1$.

(Second Embodiment)

In the first embodiment of the present invention, sapphire has been employed for the substrate **1**. However, in place of the sapphire, any other material such as, for example, Si, GaAs, GaN, SiC or a heat-resistant glass (a glass of a kind which does not soften at the temperature at which the selective growth of the GaN layer takes place) may be employed for the substrate **1**.

Such a substrate is advantageous in many aspects, for example, inexpensive and easy to handle.

Even where any of those alternative materials is employed for the substrate **1**, the step of crystalline growth is substantially similar to that described in connection with the foregoing embodiment and the substrate can have an electrical conductivity if appropriate impurities are added.

It is to be noted that even where Si, GaAs, or the like is employed for the substrate, crystal orientation of the substrate is not limited to a particular direction as is the case with the sapphire substrate.

(Third Embodiment)

FIGS. **6** and **7** illustrate cross-sectional representations of GaN layers formed according to a third embodiment of the present invention.

This third embodiment of the present invention differs from the embodiment shown in FIG. **1** in that as shown in FIGS. **6** and **7**, neither the low temperature buffer layer **2** nor the GaN layer **3**, such as shown in FIG. **1**, is formed and, instead, the dielectric mask **4** is formed directly on the substrate **1**, followed by successive lamination of the GaN layer **5** and the AlN layer **6**. Also, while in FIG. **6** the GaN layer is first formed directly on the substrate **1**, in FIG. **7** the AlN layer **7** is formed directly on the substrate **1**.

Thus, even though neither of the buffer layer **2** nor the GaN layer **3** is formed, it is possible to form the GaN layer 5^{n+1} having a minimized deterioration in surface morphology and also having a minimized density of defects as is the case with the foregoing embodiments of the present invention.

It is to be noted that, in place of the GaN layer 5, 5', . . . and 5^{n+1}, different GaN-type compound layers expressed by the following formula can be equally employed:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$.

Also, in place of the thin AlN layers 6, 6', . . . and 6^n, AlN-type thin layers prepared from a composition containing a relatively high quantity of Al, which is expressed by the following formula may be employed:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq 1$.

(Fourth Embodiment)

FIGS. **8A** to **8D** illustrate the sequence of manufacture of a ridge-type (stripe-type) laser on the GaN layer according to the present invention.

In the first place, as shown in FIG. **8A**, an n-type GaN clad layer **3**, an active layer **9**, and a p-type GaN clad layer **10** are

successively deposited on the high-quality GaN compound layer formed in the manner as described in connection with the first embodiment of the present invention. The active layer **9** includes a multi-quantum well of InGaN/AlGaN layers for emission of a laser beam, sandwiched between the GaN clad layers **8** and **10**, to form a p-n junction of a double-hetero (DH) structure.

Subsequently, as shown in FIG. **8**B, in order to form the ridge structure, the n-type GaN clad layer **8**, the active layer **9** and the p-type GaN clad layer **10** are etched by the use of any known lithographic technique and a dry etching technique.

Then, as shown in FIG. **8**C, after a protective film **13** of, for example, SiO_2 has been deposited on a side wall of the ridge, an opening is formed by the use of a lithographic technique and etching.

Finally, as shown in FIG. **8**D, metal contacts **11** and **12** are formed and a mirror facet (not shown) is formed for defining a cavity.

In this way, by forming a laser structure on the high-quality GaN layer formed according to the present invention, it is possible to improve the device characteristic, to increase lifetime, and to lower the threshold current density and power consumption.

It is to be noted that each of the layers **8** to **10** may be prepared from different GaN-type compound layers expressed by the following formula can be equally employed:

$$Ga_xAl_yIn_zN \qquad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+y+z=1$.

Also, in place of the high-quality GaN layer shown in connection with the first embodiment of the present invention, the substrate and the structure both shown in connection with the second embodiment of the present invention can be equally employed.

(Fifth Embodiment)

FIG. **9** illustrates a cross-sectional view of the high-quality GaN layer applied to a surface emitting laser (VSCEL: Vertical Cavity Surface Emitting Laser).

In this embodiment, a lower Bragg reflection layer structure **14**, an active layer and a cavity **15**, and an upper Bragg reflection layer structure **16** are successively deposited on the high-quality GaN layer shown in connection with the first embodiment of the present invention.

The lower Bragg reflection layer structure **14** is in the form of a multi-layered structure of AlN/AlGaN layers each having a film thickness within the range of 20 to 50 nm, depending on the composition and the wavelength of light emitted, and is operable to reflect the laser beam partly back into the cavity.

The cavity and active layer **15** are of a laser structure including a p-n junction and InGaN/AlGaN quantum well layers. The upper Bragg reflection layer structure **113** is in the form of a layer of nitride compound crystals or a multi-layered structure such as, for example, SiO_2/MgO or SiO_2/ZrO_2. More preferably, the Bragg reflection layer structure **14** is made up of AlN/GaN multi-layered structures 5, 6 . . . .

It is to be noted that although J. Redwings et al. have published the use of $Al_{0.4}Ga_{0.6}N/Al_{0.12}Ga_{0.88}N$ (39.7 nm/37.2 nm) of 30 cycles for the Bragg reflection layer structure **14**, no favorable characteristic is obtained because of poor crystalline quality.

In the present invention, however, since the Bragg reflection layer structure **14** is formed over the high-quality GaN crystal, any possible deterioration of the laser characteristic due to the poor crystalline quality can be considerably suppressed.

(Sixth Embodiment)

FIG. **10** illustrates a cross-sectional representation of the high-quality GaN layer applied to an ultraviolet (UV) light detector.

The crystal quality of the device plays an important role in the underwater communication, in the ground-to-space communication at high frequency operation, or in a UV detector such as a combustion detector. In other words, the performance of the UV detector referred to above can be improved by the use of the high-quality GaN layer of the present invention.

The UV detector according to this embodiment of the present invention includes, as shown in FIG. **10**, an n-GaN layer (or n-$Al_xGa_{1-x}N$ ($0\leqq x\leqq 1$) layer) **8** and a p-GaN layer (or n-$Al_xGa_{1-x}N$ ($0\leqq x\leqq 1$) layer) **10** both formed on the high-quality GaN layer with a transparent contact **1** and another contact **12** being formed on the p-GaN layer **10** and the n-GaN layer **8**, respectively.

FIG. **11** shows a cross-sectional representation of the high-quality GaN layer applied to a GaN/AlGaN HFET that can be generally used as UV photodetector device.

The GaN/AlGaN HFET is formed by depositing successively on the high-quality GaN layer **5"** of the present invention, an undoped GaN layer **8**, an n-AlGaN barrier layer **18** doped with $n=4\times10^{18}$ cm^{-3} and having a film thickness of 25 nm, a metal gate 19 of 0.2 μm in gate length, and a source, a drain contact **17**.

In this GaN/AlGaN HFET, electron-hole pairs are generated inside the GaN layer **8** with the electrons and the holes migrating respectively towards a channel and the substrate.

Accordingly, by the use of the high-quality GaN crystal of the present invention, it is possible to increase the sensitivity and also to improve the device characteristics such as increasing of the operating frequency to a high band region due to a reduction in the number of traps.

(Seventh Embodiment)

The seventh embodiment of the present invention lies in application of the high-quality GaN layer of the present invention to an HFET, a cross-sectional structure of which is shown in FIG. **11** and is similar to that shown in connection with the sixth embodiment of the present invention. The crystal quality of the GaN layer is an important factor because it affects the high frequency characteristic of the transistor and, particularly, application to a microwave element.

Accordingly, the formation of the high-quality GaN layer of the present invention in the HFET is effective to considerably improve the transistor characteristic of the HFET.

It is to be noted that even any other electronic device such as HBT, HEMT or FET can have an improved element characteristic if formed on the high-quality GaN layer of the present invention. For example, the lifetime of carriers can be increased, the operating frequency can be increased and loss of the electrical power can be reduced.

It is to be noted that in any one of the fourth to seventh embodiments of the present invention, the substrate and the structure shown in connection with any one of the second and third embodiments of the present invention can be employed in place of the high-quality GaN layer shown in connection with the first embodiment of the present invention.

From the foregoing full description of the various preferred embodiments of the present invention, it has now become clear that with the selective growing method to form the gallium nitride layer of the present invention, the aluminum nitride thin layer effective to increase the length of migration of the Ga atoms as compared with that of the

gallium nitride layer is suitably interposed between each neighboring gallium nitride layers which are selectively grown to thereby accomplish a flattening of the gallium nitride layer immediately above the aluminum nitride thin layer. Accordingly, not only can the surface irregularities present at the surface of the substrate laminated with the gallium nitride layer be reduced, but also it is possible a GaN-type layer excellent in surface flatness.

Also, since the aluminum nitride thin layer serves to trap the screw dislocations occurring in the gallium nitride layer immediately beneath the aluminum nitride thin layer to thereby avoid propagation to the gallium nitride layer immediately thereabove, the consequence is that the defect density at the surface of the substrate laminated with the GaN layer can be reduced.

In addition, the use of the high-quality gallium nitride layer of the present invention is effective to increase the yield of manufacture of devices to be formed on the substrate laminated with the gallium nitride layer because the substrate laminated with the gallium nitride layer has an excellent surface crystal quality.

Yet, because of the reduced defect density of the substrate laminated with the gallium nitride layer, it is also possible to increase the characteristics and the reliability of elements formed on the substrate.

Although the present invention has been described in connection with the preferred embodiments thereof, it should be noted that various changes and modifications are apparent to those skilled in the art. Accordingly, such changes and modifications so far as encompassed by the appended claims are to be understood as included within the scope of the present invention.

What is claimed is:

1. A substrate laminated with a high-quality gallium nitride layer comprising:

a substrate;

a dielectric mask on the substrate and having a surface partially exposed at an opening;

a plurality of gallium nitride selectively grown layers, each grown on a portion of the substrate encompassed by the opening, each said gallium nitride selectively grown layer having a composition expressed by the chemical formula:

$$Ga_xAl_yIn_zN \quad (I)$$

wherein $0<x\leqq 1$, $0\leqq y<1$, $0\leqq z<1$, and $x+Y+z=1$; and

an aluminum nitride thin layer interposed between pairs of neighboring gallium nitride selectively grown layers, said aluminum nitride layer having a composition expressed by the formula:

$$Al_xGa_{1-x}N \quad (II)$$

wherein $0.7<x\leqq 1$.

2. The substrate as claimed in claim 1, further comprising a buffer layer and gallium nitride layer formed on the substrate prior to the formation of the dielectric mask.

3. The substrate as claimed in claim 1, wherein the aluminum nitride thin layer contacts the substrate or the gallium nitride layer contacts substrate.

4. A semiconductor device which comprises:

the substrate as claimed in claim 1;

a photoelectric semiconductor element, an electronic semiconductor element or an electro-optical integrated semiconductor element.

5. The semiconductor device as claimed in claim 4, wherein a photo electric semiconductor element comprises:

a laser element region having successively deposited on the laminated substrate a stripe-shaped n-type gallium nitride clad layer, a stripe-shaped gallium nitride active layer and a p-type gallium nitride clad layer.

6. The semiconductor device as claimed in claim 4, wherein a photo electric semiconductor element comprises:

a lower Bragg reflection layer structure formed on the laminated substrate;

a n-type gallium nitride clad layer, gallium nitride active layer and p-type gallium nitride clad layer deposited successively on the lower Bragg reflection layer structure;

a laser element region including an upper Bragg reflection layer structure formed over the p-type gallium nitride clad layer.

7. The semiconductor device as claimed in claim 6, wherein a laminated structure including the gallium nitride layer and the aluminum nitride thin layer on the laminated substrate concurrently serves as the lower Bragg reflection layer structure.

8. The semiconductor device as claimed in claim 4, wherein a photoelectric semiconductor element comprises:

a detector element region having successively deposited on the laminated substrate a n-type gallium nitride clad layer and a p-type gallium nitride clad layer.

* * * * *

US006177688B1

(12) **United States Patent**
Linthicum et al.

(10) **Patent No.: US 6,177,688 B1**
(45) **Date of Patent: Jan. 23, 2001**

(54) **PENDEOEPITAXIAL GALLIUM NITRIDE SEMICONDUCTOR LAYERS ON SILCON CARBIDE SUBSTRATES**

(75) Inventors: **Kevin J. Linthicum**, Angier; **Thomas Gehrke**, Carrboro; **Darren B. Thomson**, Cary; **Eric P. Carlson**, Raleigh; **Pradeep Rajagopal**, Raleigh; **Robert F. Davis**, Raleigh, all of NC (US)

(73) Assignee: **North Carolina State University**, Raleigh, NC (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/198,784**

(22) Filed: **Nov. 24, 1998**

(51) **Int. Cl.**[7] **H01L 29/267**

(52) **U.S. Cl.** **257/77**; 257/76; 257/190; 257/201

(58) **Field of Search** 257/76, 77, 190, 257/201

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Primary Examiner—Gene M. Munson
(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec

(57) **ABSTRACT**

An underlying gallium nitride layer on a silicon carbide substrate is masked with a mask that includes an array of openings therein, and the underlying gallium nitride layer is etched through the array of openings to define posts in the underlying gallium nitride layer and trenches therebetween. The posts each include a sidewall and a top having the mask thereon. The sidewalls of the posts are laterally grown into the trenches to thereby form a gallium nitride semiconductor layer. During this lateral growth, the mask prevents nucleation and vertical growth from the tops of the posts. Accordingly, growth proceeds laterally into the trenches, suspended from the sidewalls of the posts. The sidewalls of the posts may be laterally grown into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer. The lateral growth from the sidewalls of the posts may be continued so that the gallium nitride layer grows vertically through the openings in the mask and laterally overgrows onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer. The lateral overgrowth can be continued until the grown sidewalls coalesce on the mask to thereby form a continuous gallium nitride semiconductor layer. Microelectronic devices may be formed in the continuous gallium nitride semiconductor layer.

22 Claims, 4 Drawing Sheets

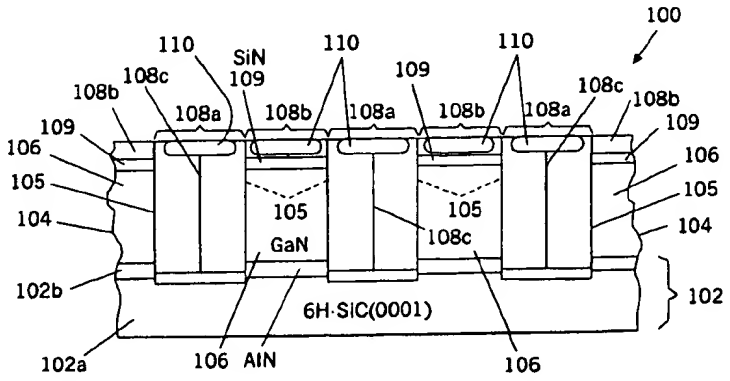

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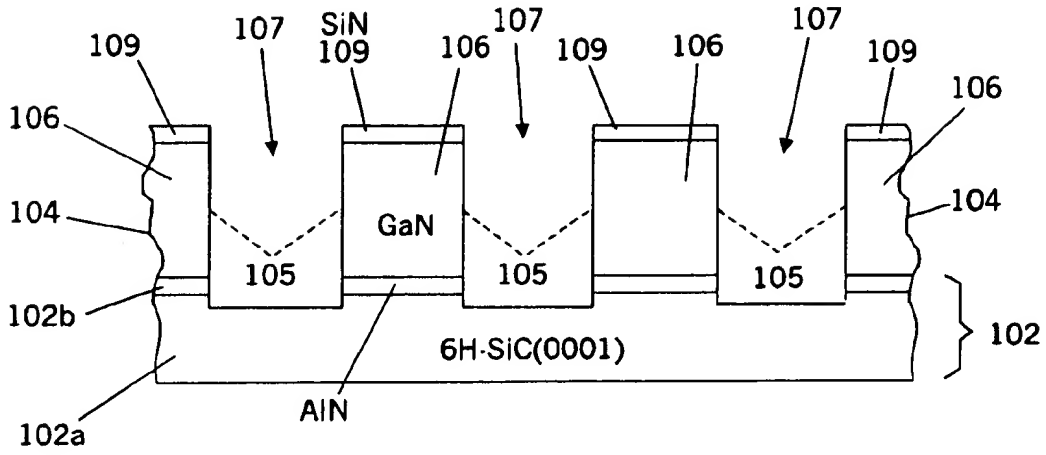
FIG. 1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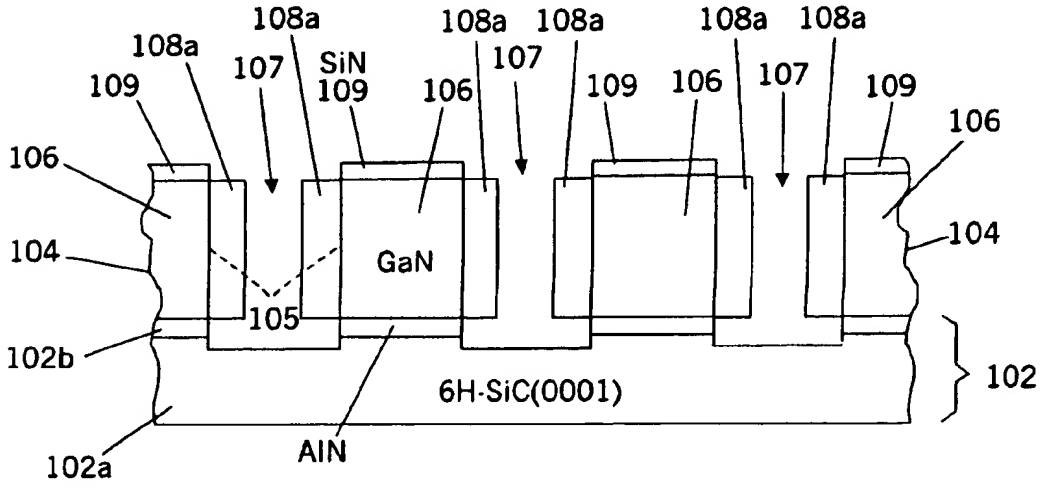
AlN
102a

FIG. 2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102b
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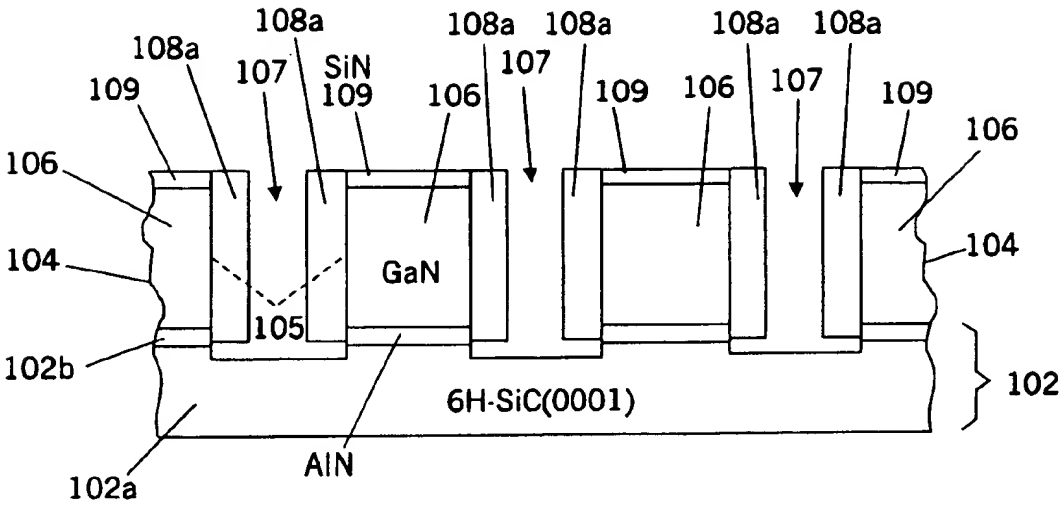
AlN
102a

FIG. 3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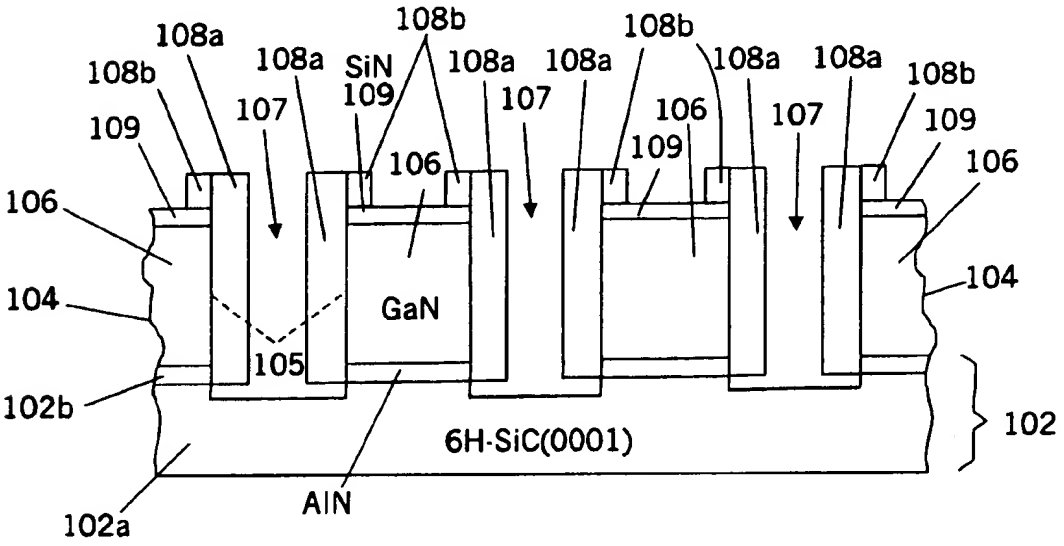
AlN
102a

FIG. 4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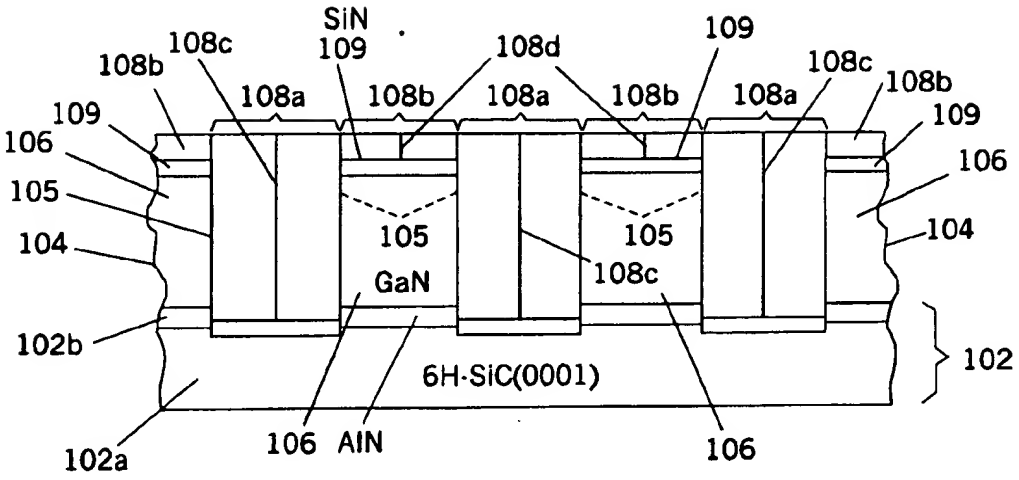
AlN
102a

FIG. 5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GaN
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6H-SiC(0001)
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AlN
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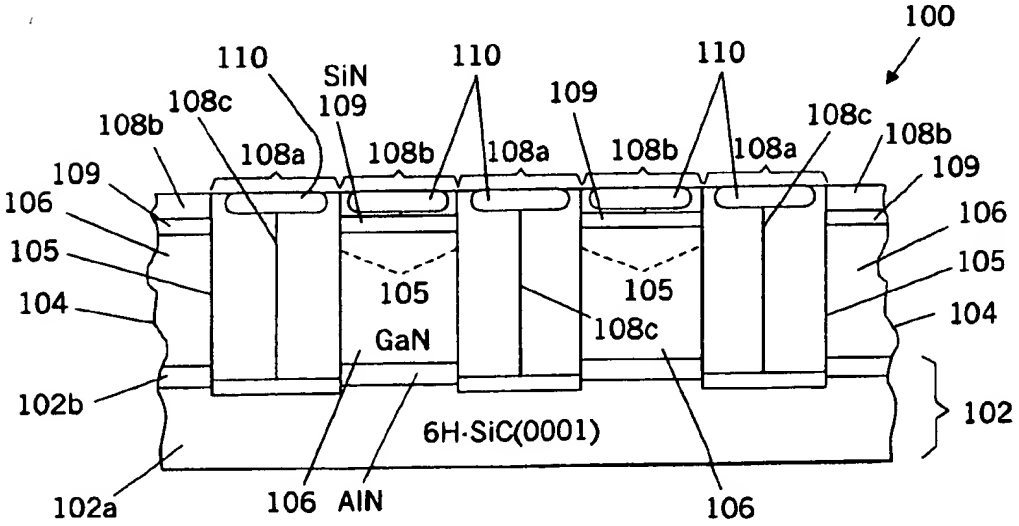
FIG. 6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AlN
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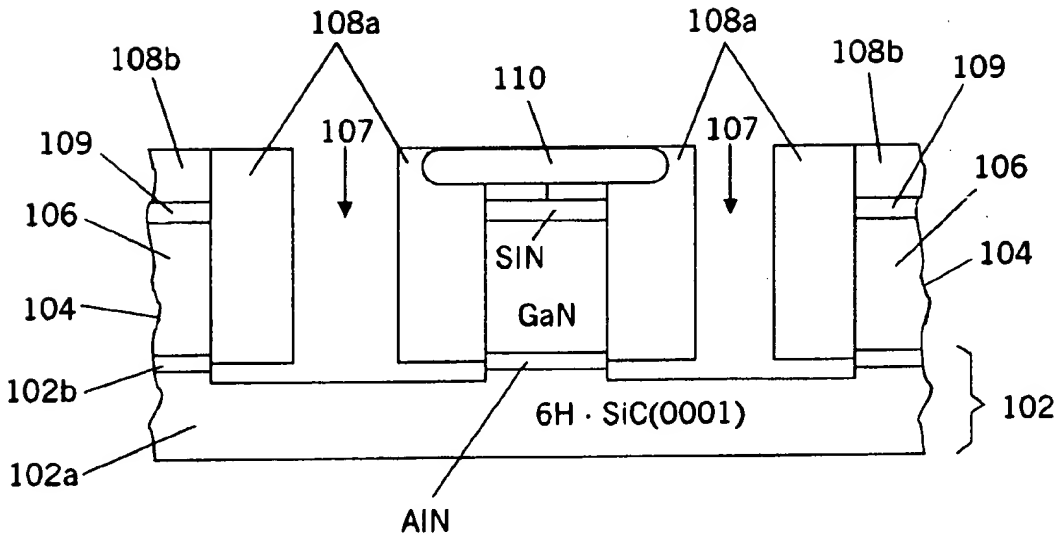
FIG. 7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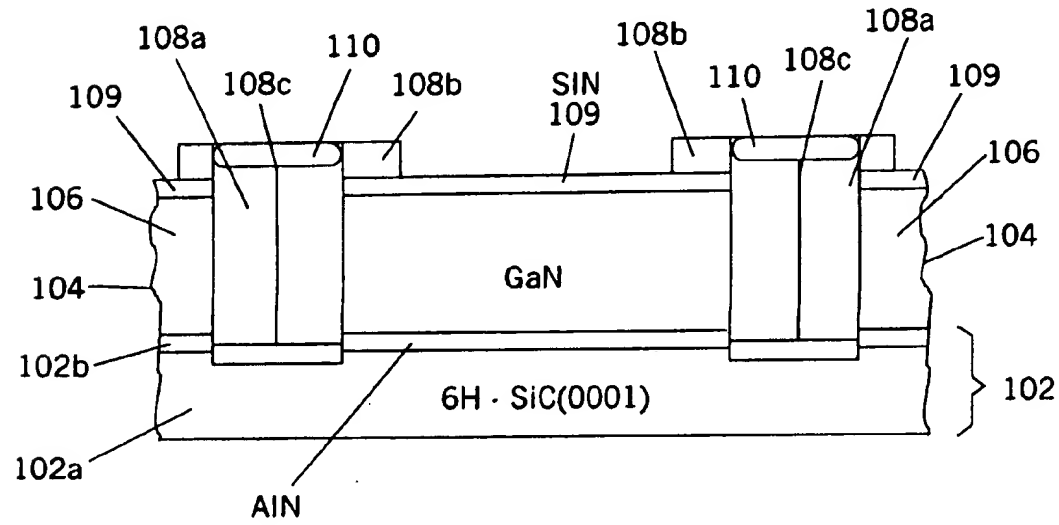
102a
AlN

FIG. 8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GaN
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102b
6H · SiC(0001)
102
102a
AlN

PENDEOEPITAXIAL GALLIUM NITRIDE SEMICONDUCTOR LAYERS ON SILCON CARBIDE SUBSTRATES

FEDERALLY SPONSORED RESEARCH

This invention was made with Government support under Office of Naval Research Contract Nos. N00014-96-1-0765, N00014-98-1-0384, and N00014-98-1-0654. The Government may have certain rights to this invention.

FIELD OF THE INVENTION

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

BACKGROUND OF THE INVENTION

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It is also known to fabricate gallium nitride structures through openings in a mask. For example, in fabricating field emitter arrays, it is known to selectively grow gallium nitride on stripe or circular patterned substrates. See, for example, the publications by Nam et al. entitled "Selective Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on 0GaN/AlN/6H—SiC (0001) Multilayer Substrates Via Organometallic Vapor Phase Epitaxy", Proceedings of the Materials Research Society, December 1996, and "Growth of GaN and $Al_{0.2}Ga_{0.8}N$ on Patterened Substrates via Organometallic Vapor Phase Epitaxy", Japanese Journal of Applied Physics., Vol. 36, Part 2, No. 5A, May 1997, pp. L532–L535. As disclosed in these publications, undesired ridge growth or lateral overgrowth may occur under certain conditions.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide improved methods of fabricating gallium nitride semiconductor layers, and improved gallium nitride layers so fabricated.

It is another object of the invention to provide methods of fabricating gallium nitride semiconductor layers that can have low defect densities, and gallium nitride semiconductor layers so fabricated.

These and other objects are provided, according to the present invention, by masking an underlying gallium nitride layer on a silicon carbide substrate with a mask that includes an array of openings therein and etching the underlying gallium nitride layer through the array of openings to define a plurality of posts in the underlying gallium nitride layer and a plurality of trenches therebetween. The posts each include a sidewall and a top having the mask thereon. The sidewalls of the posts are laterally grown into the trenches to thereby form a gallium nitride semiconductor layer. During this lateral growth, the mask prevents nucleation and vertical growth from the tops of the posts. Accordingly, growth proceeds laterally into the trenches, suspended from the sidewalls of the posts. This form of growth is referred to herein as pendeoepitaxy from the Latin "to hang" or "to be suspended". Microelectronic devices may be formed in the gallium nitride semiconductor layer.

According to another aspect of the invention, the sidewalls of the posts are laterally grown into the trenches until the laterally grown sidewalls coalesce in the trenches to thereby form a gallium nitride semiconductor layer. The lateral growth from the sidewalls of the posts may be continued so that the gallium nitride layer grows vertically through the openings in the mask and laterally overgrows onto the mask on the tops of the posts, to thereby form a gallium nitride semiconductor layer. The lateral overgrowth can be continued until the grown sidewalls coalesce on the mask to thereby form a continuous gallium nitride semiconductor layer. Microelectronic devices may be formed in the continuous gallium nitride semiconductor layer.

It has been found, according to the present invention, that dislocation defects do not significantly propagate laterally from the sidewalls of the posts, so that the laterally grown sidewalls of the posts are relatively defect-free. Moreover, during growth, it has been found that significant vertical growth on the top of the posts is prevented by the mask so that relatively defect-free lateral growth occurs from the sidewalls onto the mask. Significant nucleation on the top of the posts also preferably is prevented. The overgrown gallium nitride semiconductor layer is therefore relatively defect-free.

Accordingly, the mask functions as a capping layer on the posts that forces the selective homoepitaxial growth of gallium nitride to occur only on the sidewalls. Defects associated with heteroepitaxial growth of the gallium nitride seed layer are pinned under the mask. By using a combination of growth from sidewalls and lateral overgrowth, a complete coalesced layer of relatively defect-free gallium nitride may be fabricated over the entire surface of a wafer in one regrowth step.

The pendeoepitaxial gallium nitride semiconductor layer may be laterally grown using metalorganic vapor phase epitaxy (MOVPE). For example, the lateral gallium nitride layer may be laterally grown using triethylgallium (TEG) and ammonia (NH_3) precursors at about 1000–1100° C. and about 45 Torr. Preferably, TEG at about 13–39 μmol/min and NH_3 at about 1500 sccm are used in combination with about 3000 sccm H_2 diluent. Most preferably, TEG at about 26 μmol/min, NH_3 at about 1500 sccm and H_2 at about 3000 sccm at a temperature of about 1100° C. and about 45 Torr are used. The underlying gallium nitride layer preferably is formed on a substrate such as 6H—SiC(0001), which itself includes a buffer layer such as aluminum nitride thereon. Other buffer layers such as gallium nitride may be used. Multiple substrate layers and buffer layers also may be used.

The underlying gallium nitride layer including the sidewall may be formed by forming trenches in the underlying gallium nitride layer, such that the trenches define the sidewalls. Alternatively, the sidewalls may be formed by forming masked posts on the underlying gallium nitride layer, the masked posts including the sidewalls and defining the trenches. A series of alternating trenches and masked posts is preferably formed to form a plurality of sidewalls.

The posts are formed such that the top surface and not the sidewalls are masked. As described above, trenches and/or posts may be formed by masking and selective etching. Alternatively, selective epitaxial growth, combinations of etching and growth, or other techniques may be used. The mask may be formed on the post tops after formation of the posts. The trenches may extend into the buffer layer and/or into the substrate so that the trench floors are in the buffer layer and preferably are in the silicon carbide substrate.

The sidewalls of the posts in the underlying gallium nitride layer are laterally grown into the trenches, to thereby form a lateral gallium nitride layer of lower defect density than that of the underlying gallium nitride layer. Some vertical growth may also occur in the trenches, although vertical growth from the post tops is reduced and preferably suppressed by the mask thereon. The laterally grown gallium nitride layer is vertically grown through the openings in the mask while propagating the lower defect density. As the height of the vertical growth extends through the openings in the mask, lateral growth over the mask occurs while propagating the lower defect density to thereby form an overgrown lateral gallium nitride layer on the mask.

Gallium nitride semiconductor structures according to the invention comprise a silicon carbide substrate and a plurality of gallium nitride posts on the silicon carbide substrate. The posts each include a sidewall and a top and define a plurality of trenches therebetween. A capping layer is provided on the tops of the posts. A lateral gallium nitride layer extends laterally from the sidewalls of the posts into the trenches. The lateral gallium nitride layer may also be referred to as a pendeoepitaxial gallium nitride layer. The lateral gallium nitride layer may be a continuous lateral gallium nitride layer that extends between adjacent sidewalls across the trenches therebetween.

The lateral gallium nitride layer may also extend vertically through the array of openings. An overgrown lateral gallium nitride layer may also be provided that extends laterally onto the capping layer. The overgrown lateral gallium nitride layer may be a continuous overgrown lateral gallium nitride layer that extends between the adjacent sidewalls across the capping layer therebetween.

A plurality of microelectronic devices may be provided in the lateral gallium nitride layer and/or in the overgrown lateral gallium nitride layer. A buffer layer may be included between the silicon carbide substrate and the plurality of posts. The trenches may extend into the silicon carbide substrate, into the buffer layer or through the buffer layer and into the silicon carbide substrate. The gallium nitride posts may be of a defect density, and the lateral gallium nitride layer and the overgrown lateral gallium nitride layer are of lower defect density than the defect density. Accordingly, low defect density gallium nitride semiconductor layers may be produced, to thereby allow the production of high performance microelectronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1–6** are cross-sectional views of gallium nitride semiconductor structures during intermediate fabrication steps according to the present invention.

FIGS. **7** and **8** are cross-sectional views of other embodiments of gallium nitride semiconductor structures according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or "onto" another element, it can be directly on the other element or intervening elements may also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to FIGS. **1–6**, methods of fabricating gallium nitride semiconductor structures according to the present invention will now be described. As shown in FIG. **1**, an underlying gallium nitride layer **104** is grown on a substrate **102**. The substrate **102** may include a 6H—SiC (0001) substrate **102***a* and an aluminum nitride or other buffer layer **102***b*. The crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further. The underlying gallium nitride layer **104** may be between 0.5 and 2.0 μm thick, and may be grown at 1000° C. on a high temperature (1100° C.) aluminum nitride buffer layer **102***b* that was deposited on the 6H-SiC substrate **102***a* in a cold wall vertical and inductively heated metalorganic vapor phase epitaxy system using triethylgallium at 26 μmol/min, ammonia at 1500 sccm and 3000 sccm hydrogen diluent. Additional details of this growth technique may be found in a publication by T. W. Weeks et al. entitled "GaN Thin Films Deposited Via Organometallic Vapor Phase Epitaxy on (6H)-SiC (0001) Using High-Temperature Monocrystalline AlN Buffer Layers", Applied Physics Letters, Vol. 67, No. 3, Jul. 17, 1995, pp. 401–403, the disclosure of which is hereby incorporated herein by reference. Other silicon carbide substrates, with or without buffer layers, may be used.

Continuing with the description of FIG. **1**, a mask such as a silicon nitride (SiN) mask **109** is included on the underlying gallium nitride layer **104**. The mask **109** may have a thickness of about 1000 Å and may be formed on the underlying gallium nitride layer **104** using low pressure chemical vapor deposition (CVD) at 410° C. The mask **109** is patterned to provide an array of openings therein, using conventional photolithography techniques.

As shown in FIG. **1**, the underlying gallium nitride layer is etched through the array of openings to define a plurality of posts **106** in the underlying gallium nitride layer **104** and a plurality of trenches **107** therebetween. The posts each include a sidewall **105** and a top having the mask **109** thereon. It will also be understood that although the posts **106** and trenches **107** are preferably formed by masking and etching as described above, the posts may also be formed by selectively growing the posts from an underlying gallium nitride layer and then forming a capping layer on the tops of the posts. Combinations of selective growth and selective etching may also be used.

Still referring to FIG. **1**, the underlying gallium nitride layer **104** includes a plurality of sidewalls **105** therein. It will be understood by those having skill in the art that the sidewalls **105** may be thought of as being defined by the plurality of spaced apart posts **106**, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls **105** may also be thought of as being defined by the plurality of trenches **107**, also referred to as "wells", in the underlying

gallium nitride layer **104**. The sidewalls **105** may also be thought of as being defined by a series of alternating trenches **107** and posts **106**. As described above, the posts **106** and the trenches **107** that define the sidewalls **105** may be fabricated by selective etching and/or selective epitaxial growth and/or other conventional techniques. Moreover, it will also be understood that the sidewalls need not be orthogonal to the substrate **102**, but rather may be oblique thereto.

It will also be understood that although the sidewalls **105** are shown in cross-section in FIG. **1**, the posts **106** and trenches **107** may define elongated regions that are straight, V-shaped or have other shapes. As shown in FIG. **1**, the trenches **107** may extend into the buffer layer **102***b* and into the substrate **102***a*, so that subsequent gallium nitride growth occurs preferentially on the sidewalls **105** rather than on the trench floors. In other embodiments, the trenches may not extend into the substrate **102***a*, and also may not extend into the buffer layer **102***b*, depending, for example, on the trench geometry and the lateral versus vertical growth rates of the gallium nitride.

Referring now to FIG. **2**, the sidewalls **105** of the underlying gallium nitride layer **104** are laterally grown to form a lateral gallium nitride layer **108***a* in the trenches **107**. Lateral growth of gallium nitride may be obtained at 1000–1100° C. and 45 Torr. The precursors TEG at 13–39 μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As used herein, the term "lateral" means a direction that is parallel to the faces of the substrate **102**. It will also be understood that some vertical growth of the lateral gallium nitride **108***a* may also take place during the lateral growth from the sidewalls **105**. As used herein, the term "vertical" denotes a directional parallel to the sidewalls **105**. However, it will be understood that growth and/or nucleation on the top of the posts **106** is reduced and is preferably eliminated by the mask **109**.

Referring now to FIG. **3**, continued growth of the lateral gallium nitride layer **108***a* causes vertical growth of the lateral gallium nitride layer **108***a* through the array of openings. Conditions for vertical growth may be maintained as was described in connection with FIG. **2**. As also shown in FIG. **3**, continued vertical growth into trenches **107** may take place at the bottom of the trenches.

Referring now to FIG. **4**, continued growth of the lateral gallium nitride layer **108***a* causes lateral overgrowth onto the mask **109**, to form an overgrown lateral gallium nitride layer **108***b*. Growth conditions for overgrowth may be maintained as was described in connection with FIG. **2**.

Referring now to FIG. **5**, growth is allowed to continue until the lateral growth fronts coalesce in the trenches **107** at the interfaces **108***c*, to form a continuous lateral gallium nitride semiconductor layer **108***a* in the trenches.

Still referring to FIG. **5**, growth is also allowed to continue until the lateral overgrowth fronts coalesce over the mask **109** at the interfaces **108***d*, to form a continuous overgrown lateral gallium nitride semiconductor layer **108***b*. The total growth time may be approximately 60 minutes. A single continuous growth step may be used. As shown in FIG. **6**, microelectronic devices **110** may then be formed in the lateral gallium nitride semiconductor layer **108***a*. Microelectronic devices also may be formed in the overgrown lateral gallium nitride layer **108***b*.

Accordingly, in FIG. **6**, gallium nitride semiconductor structures **100** according to the present invention are illustrated. The gallium nitride structures **100** include the substrate **102**. The substrate preferably includes the 6H—SiC (0001) substrate **102***a* and the aluminum nitride buffer layer **102***b* on the silicon carbide substrate **102***a*. The aluminum nitride buffer layer **102***b* may be 0.1 μm thick.

The fabrication of the substrate **102** is well known to those having skill in the art and need not be described further. Fabrication of silicon carbide substrates are described, for example, in U.S. Pat. Nos. 4,865,685 to Palmour; U.S.Pat. No. Re 34,861 to Davis et al.; U.S. Pat. No. 4,912,064 to Kong et al. and U.S. Pat. No. 4,946,547 to Palmour et al., the disclosures of which are hereby incorporated herein by reference.

The underlying gallium nitride layer **104** is also included on the buffer layer **102***b* opposite the substrate **102***a*. The underlying gallium nitride layer **104** may be between about 0.5 and 2.0 μm thick, and may be formed using metalorganic vapor phase epitaxy (MOVPE). The underlying gallium nitride layer generally has an undesired relatively high defect density. For example, dislocation densities of between about 10^8 and 10^{10} cm^{-2} may be present in the underlying gallium nitride layer. These high defect densities may result from mismatches in lattice parameters between the buffer layer **102***b* and the underlying gallium nitride layer **104**, and/or other causes. These high defect densities may impact the performance of microelectronic devices formed in the underlying gallium nitride layer **104**.

Still continuing with the description of FIG. **6**, the underlying gallium nitride layer **104** includes the plurality of sidewalls **105** that may be defined by the plurality of posts **106** and/or the plurality of trenches **107**. As was described above, the sidewalls may be oblique and of various elongated shapes. Also as was described above, the gallium nitride posts **106** are capped with a capping layer such as a mask **109**, preferably comprising silicon nitride.

Continuing with the description of FIG. **6**, the lateral gallium nitride layer **108***a* extends laterally and vertically from the plurality of sidewalls **105** of the underlying gallium nitride layer **104**. The overgrown lateral gallium nitride **108***b* extends from the lateral gallium nitride layer **108***a*. The lateral gallium nitride layer **108***a* and the overgrown lateral gallium nitride layer **108***b* may be formed using metalorganic vapor phase epitaxy at about 1000–1100° C. and about 45 Torr. Precursors of triethygallium (TEG) at about 13–39 μmol/min and ammonia (NH_3) at about 1500 sccm may be used in combination with an about 3000 sccm H_2 diluent, to form the lateral gallium nitride layer **108***a* and the overgrown lateral gallium nitride layer **108***b*.

As shown in FIG. **6**, the lateral gallium nitride layer **108***a* coalesces at the interfaces **108***c* to form a continuous lateral gallium nitride semiconductor layer **108***a* in the trenches. It has been found that the dislocation densities in the underlying gallium nitride layer **104** generally do not propagate laterally from the sidewalls **105** with the same density as vertically from the underlying gallium nitride layer **104**. Thus, the lateral gallium nitride layer **108***a* can have a relatively low dislocation defect density, for example less than about 10^4 cm^{-2}. From a practical standpoint, this may be regarded as defect-free. Accordingly, the lateral gallium nitride layer **108***a* may form device quality gallium nitride semiconductor material. Thus, as shown in FIG. **6**, microelectronic devices **110** may be formed in the lateral gallium nitride semiconductor layer **108***a*.

Still referring to FIG. **6**, the overgrown lateral gallium nitride layer **108***b* coalesces at the interfaces **108***d* to form a continuous overgrown lateral gallium nitride semiconductor

layer **108***b* over the masks. It has been found that the dislocation densities in the underlying gallium nitride layer **104** and of the lateral gallium nitride layer **108***a* generally do not propagate laterally with the same density as vertically from the underlying gallium nitride layer **104** and the lateral gallium nitride layer **108***a*. Thus, the overgrown lateral gallium nitride layer **108***b* also can have a relatively low defect density, for example less than about 10^4 cm^{-2}. Accordingly, the overgrown lateral gallium nitride layer **108***b* may also form device quality gallium nitride semiconductor material. Thus, as shown in FIG. **6**, microelectronic devices **110** may also be formed in the overgrown lateral gallium nitride semiconductor layer **108***b*.

Referring now to FIGS. **7** and **8**, other embodiments of gallium nitride semiconductor structures and fabrication methods according to the present invention will now be described. Gallium nitride structures are fabricated as was already described in connection with FIGS. **1–6** using different spacings or dimensions for the posts and trenches. In FIG. **7**, a small post-width/trench-width ratio is used to produce discrete gallium nitride structures. In FIG. **8**, a large post-width/trench-width ratio is used, to produce other discrete gallium nitride structures.

Referring now to FIG. **7**, using a small post-width/trench-width ratio, gallium nitride semiconductor structures of FIG. **7** are fabricated as was already described in connection with FIGS. **1–4**. Still referring to FIG. **7**, growth is allowed to continue until the overgrown lateral fronts coalesce over the mask **109** at the interfaces **108***d*, to form a continuous overgrown lateral gallium nitride semiconductor layer over the mask **109**. The total growth time may be approximately 60 minutes. As shown in FIG. **7**, microelectronic devices **110** may be formed in the overgrown lateral gallium nitride layer **108***b*.

Referring now to FIG. **8**, using a large post-width/trench-width ratio, gallium nitride semiconductor structures of FIG. **8** are fabricated as was already described in connection with FIG. **1–4**. Still referring to FIG. **8**, growth is allowed to continue until the overgrown lateral fronts coalesce in the trenches **107** at the interfaces **108***c*, to form a continuous gallium nitride semiconductor layer **108***a* in the trenches **107**. The total growth time may be approximately 60 minutes. As shown in FIG. **8**, microelectronic devices **110** may be formed in the pendeoepitaxial gallium nitride layer **108***a*.

Additional discussion of methods and structures of the present invention will now be provided. The trenches **107** and are preferably rectangular trenches that preferably extend along the <11$\bar{2}$0> and/or <1$\bar{1}$00> directions on the underlying gallium nitride layer **104**. Truncated triangular stripes having (1$\bar{1}$01) slant facets and a narrow (0001) top facet may be obtained for trenches along the <11$\bar{2}$0> direction. Rectangular stripes having a (0001) top facet, (11$\bar{2}$0) vertical side faces and (1$\bar{1}$01) slant facets may be grown along the <1$\bar{1}$00> direction. For growth times up to 3 minutes, similar morphologies may be obtained regardless of orientation. The stripes develop into different shapes if the growth is continued.

The amount of lateral growth generally exhibits a strong dependence on trench orientation. The lateral growth rate of the <1$\bar{1}$00> oriented is generally much faster than those along <11$\bar{2}$0>. Accordingly, it is most preferred to orient the trenches so that they extend along the <1$\bar{1}$00> direction of the underlying gallium nitride layer **104**.

The different morphological development as a function of orientation appears to be related to the stability of the crystallographic planes in the gallium nitride structure. Trenches oriented along <11$\bar{2}$0> may have wide (1$\bar{1}$00) slant facets and either a very narrow or no (0001) top facet depending on the growth conditions. This may be because (1$\bar{1}$01) is the most stable plane in the gallium nitride wurtzite crystal structure, and the growth rate of this plane is lower than that of others. The {1$\bar{1}$01} planes of the <1$\bar{1}$00> oriented trenches may be wavy, which implies the existence of more than one Miller index. It appears that competitive growth of selected {1$\bar{1}$01} planes occurs during the deposition which causes these planes to become unstable and which causes their growth rate to increase relative to that of the (1$\bar{1}$01) of trenches oriented along <11$\bar{2}$0>.

The morphologies of the gallium nitride layers selectively grown from trenches oriented along <1$\bar{1}$00> are also generally a strong function of the growth temperatures. Layers grown at 1000° C. may possess a truncated triangular shape. This morphology may gradually change to a rectangular cross-section as the growth temperature is increased. This shape change may occur as a result of the increase in the diffusion coefficient and therefore the flux of the gallium species along the (0001) top plane onto the {1$\bar{1}$01} planes with an increase in growth temperature. This may result in a decrease in the growth rate of the (0001) plane and an increase in that of the {1$\bar{1}$01}. This phenomenon has also been observed in the selective growth of gallium arsenate on silicon dioxide. Accordingly, temperatures of 1100° C. appear to be most preferred.

The morphological development of the gallium nitride regions also appears to depend on the flow rate of the TEG. An increase in the supply of TEG generally increases the growth rate in both the lateral and the vertical directions. However, the lateral/vertical growth rate ratio decrease from about 1.7 at the TEG flow rate of about 13 μmol/min to 0.86 at about 39 μmol/min. This increased influence on growth rate along <0001> relative to that of <11$\bar{2}$0> with TEG flow rate may be related to the type of reactor employed, wherein the reactant gases flow vertically and perpendicular to the substrate. The considerable increase in the concentration of the gallium species on the surface may sufficiently impede their diffusion to the {1$\bar{1}$01} planes such that chemisorption and gallium nitride growth occur more readily on the (0001) plane.

Continuous 2 μm thick gallium nitride semiconductor layers may be obtained using 7 μm wide trenches spaced 3 μm apart and oriented along <1$\bar{1}$00>, at about 1100° C. and a TEG flow rate of about 26 μmol/min. Continuous 2 μm thick gallium nitride semiconductor layers may also be obtained using 3 μm wide trenches spaced 2 μm apart and oriented along <1$\bar{1}$00>, also at about 1100° C. and a TEG flow rate of about 26 μmol/min. The continuous gallium nitride semiconductor layers may include subsurface voids that form when two growth fronts coalesce. These voids may occur most often using lateral growth conditions wherein rectangular trenches and/or mask openings having vertical {11$\bar{2}$0} side facets developed.

The continuous gallium nitride semiconductor layers may have a microscopically flat and pit-free surface. The surfaces of the laterally grown gallium nitride layers may include a terrace structure having an average step height of 0.32 nm. This terrace structure may be related to the laterally grown gallium nitride, because it is generally not included in much larger area films grown only on aluminum nitride buffer layers. The average RMS roughness values may be similar to the values obtained for the underlying gallium nitride layer **104**.

Threading dislocations, originating from the interface between the underlying gallium nitride layer **104** and the

buffer layer **102***b*, appear to propagate to the top surface of the underlying gallium nitride layer **104**. The dislocation density within these regions is approximately 10^9 cm^{-2}. By contrast, threading dislocations do not appear to readily propagate laterally. Rather, the lateral gallium nitride layer **108***a* and the overgrown lateral gallium nitride layer **108***b* contain only a few dislocations. In the lateral gallium nitride layer **108***a*, the few dislocations may be formed parallel to the (0001) plane via the extension of the vertical threading dislocations after a 90° bend in the regrown region. These dislocations do not appear to propagate to the top surface of the overgrown gallium nitride layer.

As described, the formation mechanism of the selectively grown gallium nitride layers is lateral epitaxy. The two main stages of this mechanism are lateral (or pendeoepitaxial) growth and lateral overgrowth. During pendeoepitaxial growth, the gallium nitride grows simultaneously both vertically and laterally. The deposited gallium nitride grows selectively on the sidewalls more rapidly than it grows on the mask **109**, apparently due to the much higher sticking coefficient, s, of the gallium atoms on the gallium nitride sidewall surface (s=1) compared to on the mask (s<<1) and substrate (s<1). Ga or N atoms should not readily bond to the mask and substrate surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would either evaporate or diffuse along the mask and substrate surface to the ends of the mask or substrate and onto the sidewalls. During lateral overgrowth, the gallium nitride also grows simultaneously both vertically and laterally. Once the pendeoepitaxial growth emerges over the masks, Ga or N atoms should still not readily bond to the mask surface in numbers and for a time sufficient to cause gallium nitride nuclei to form. They would still either evaporate or diffuse along the mask to the ends of the mask and onto the pendeoepitaxial gallium nitride vertical surfaces.

Surface diffusion of gallium and nitrogen on the gallium nitride may play a role in gallium nitride selective growth. The major source of material appears to be derived from the gas phase. This may be demonstrated by the fact that an increase in the TEG flow rate causes the growth rate of the (0001) top facets to develop faster than the $(1\bar{1}01)$ side facets and thus controls the lateral growth.

In conclusion, pendeoepitaxial and lateral epitaxial overgrowth may be obtained from sidewalls of an underlying masked gallium nitride layer via MOVPE. The growth may depend strongly on the sidewall orientation, growth temperature and TEG flow rate. Coalescence of pendeoepitaxial grown and lateral overgrown gallium nitride regions to form regions with both extremely low densities of dislocations and smooth and pit-free surfaces may be achieved through 3 μm wide trenches between 2 μm wide posts and extending along the $<1\bar{1}00>$ direction, at about 1100° C. and a TEG flow rate of about 26 μmol/min. The pendeoepitaxial and lateral overgrowth of gallium nitride from sidewalls via MOVPE may be used to obtain low defect density regions for microelectronic devices over the entire surface of the thin film.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A gallium nitride semiconductor structure, comprising:

a silicon carbide substrate;

a plurality of gallium nitride posts on the silicon carbide substrate, the posts each including a sidewall and a top, and defining a plurality of trenches therebetween;

a capping layer on the tops of the posts; and

a lateral gallium nitride layer that extends laterally from the sidewalls of the posts into the trenches, wherein the posts are of a defect density and wherein the lateral gallium nitride layer is of lower defect density than the defect desity.

2. A structure according to claim **1** wherein the lateral gallium nitride layer is a continuous lateral gallium nitride layer that extends between adjacent sidewalls across the trenches therebetween.

3. A structure according to claim **1** wherein the lateral gallium nitride layer also extends vertically in the trenches, to beyond the capping layer.

4. A structure according to claim **3** further comprising a plurality of microelectronic devices in the lateral gallium nitride layer that extends vertically in the trenches, beyond the capping layer.

5. A structure according to claim **1** further comprising a plurality of microelectronic devices in the lateral gallium nitride layer.

6. A structure according to claim **1** further comprising a buffer layer between the silicon carbide substrate and the plurality of posts.

7. A structure according to claim **6** wherein the trenches extend through the buffer layer and into the silicon carbide substrate.

8. A structure according to claim **1** wherein the trenches extend into the silicon carbide substrate.

9. A structure according to claim **1** further comprising:

a microelectronic device in the lateral gallium nitride layer.

10. A structure according to claim **1** wherein the sidewall is orthogonal to the silicon carbide substrate.

11. A structure according to claim **1** wherein the sidewall is oblique to the silicon carbide substrate.

12. A structure according to claim **1** wherein the trenches include trench floors and wherein the lateral gallium nitride layer is a cantilevered lateral gallium nitride layer that extends laterally from the sidewalls of the posts into the trenches and is spaced apart from the trench floors.

13. A gallium nitride semiconductor structure, comprising:

a silicon carbide substrate;

a plurality of gallium nitride posts on the silicon carbide substrate, the posts each including a sidewall and a top, and defining a plurality of trenches therebetween;

a capping layer on the tops of the posts;

a lateral gallium nitride layer that extends laterally from the sidewalls of the posts into the trenches and that also extends vertically in the trenches, to beyond the capping layer; and

an overgrown lateral gallium nitride layer that extends laterally from the lateral gallium nitride layer onto the capping layer, wherein the posts are of a defect density and wherein the lateral gallium nitride layer and the overgrown lateral gallium nitride layer are of lower defect density than the defect density.

14. A structure according to claim 13 wherein the overgrown lateral gallium nitride layer is a continuous overgrown lateral gallium nitride layer that extends between adjacent sidewalls across the capping layer therebetween.

15. A structure according to claim 13 further comprising a plurality of microelectronic devices in the overgrown lateral gallium nitride layer.

16. A structure according to claim 13 further comprising a buffer layer between the silicon carbide substrate and the plurality of posts.

17. A structure according to claim 16 wherein the trenches extend through the buffer layer and into the silicon carbide substrate.

18. A structure according to claim 13 wherein the trenches extend into the silicon carbide substrate.

19. A structure according to claim 16 further comprising:

a microelectronic device in the overgrown lateral gallium nitride layer.

20. A structure according to claim 13 wherein the sidewall is orthogonal to the silicon carbide substrate.

21. A structure according to claim 13 wherein the sidewall is oblique to the silicon carbide substrate.

22. A structure according to claim 13 wherein the trenches include trench floors and wherein the lateral gallium nitride layer is a cantilevered lateral gallium nitride layer that extends laterally from the sidewalls of the posts into the trenches and is spaced apart from the trench floors.

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